

# HuaQin Confidential

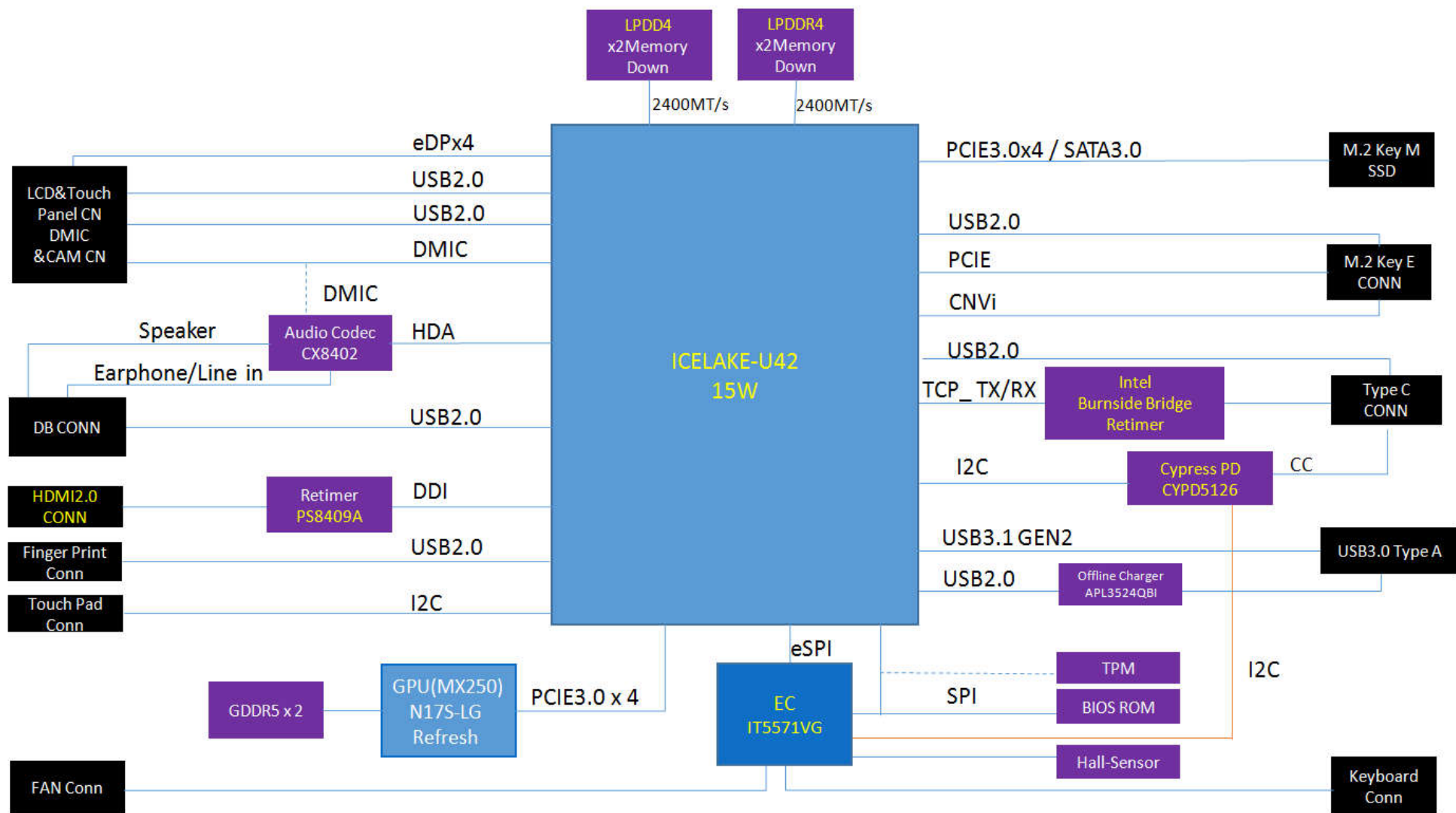
## NB8511/12\_M/B Schematics Document

### Intel ICL Lake U-Processor with LPDDR4

### REV1.0

### 2019-02-01

|          |                         |                                                                                                                                  |                             |           |
|----------|-------------------------|----------------------------------------------------------------------------------------------------------------------------------|-----------------------------|-----------|
| Author   | Leo.Liu & Payne.Zhang   |  <b>Huaqin Telecom Technology Com.,Ltd.</b> |                             |           |
| Reviewer | Nelosn.Hai & Nemo.Jiang | Page name: <b>Cover page</b>                                                                                                     |                             |           |
| Approver | Lobo_Fan                | Size: A4                                                                                                                         | Project Name: <b>NB8511</b> | REV: V1.0 |
|          |                         | Date: Monday, July 15, 2019                                                                                                      | Sheet: 1                    | of 72     |



### MEM ID

| HW_ID3 | HW_ID2 | HW_ID1 | HW_ID0 | Description                                                | Total |
|--------|--------|--------|--------|------------------------------------------------------------|-------|
| 0      | 0      | 0      | 0      | SAMSUNG LPDDR4 3733 1GB K4F8E304HB-MGCJ LF+HF D20          | 4GB   |
| 0      | 0      | 0      | 1      | HYNIX LPDDR4 3733 1GB H9HCNNN8KUMLHR-NME LF+HF DDP         | 4GB   |
| 0      | 0      | 1      | 0      | MICRON LPDDR4 4266 2GB MT53E512M32D2NP-046 WT:E LF+HF Z11N | 8GB   |
| 0      | 1      | 0      | 0      | HYNIX LPDDR4 3733 2GB H9HCNNNBPUMLHR-NME LF+HF DE          | 8GB   |
| 0      | 1      | 0      | 0      |                                                            | 16GB  |
| 1      | 0      | 0      | 0      | HYNIX LPDDR4X 4266 4GB H9HCNNNCFMALHR-NEE LF+HF QDP        |       |
|        |        |        |        | 4x 16Gb(reserve)                                           |       |

### GPU ID

| HW_ID5 | HW_ID4 | Description    |        |
|--------|--------|----------------|--------|
|        |        | N17-LG-Refresh | N17-LG |
| 0      | 0      | NC             | NC     |
| 1      | 0      | Mount          |        |
| 1      | 1      |                | Mount  |
|        |        |                |        |
|        |        |                |        |

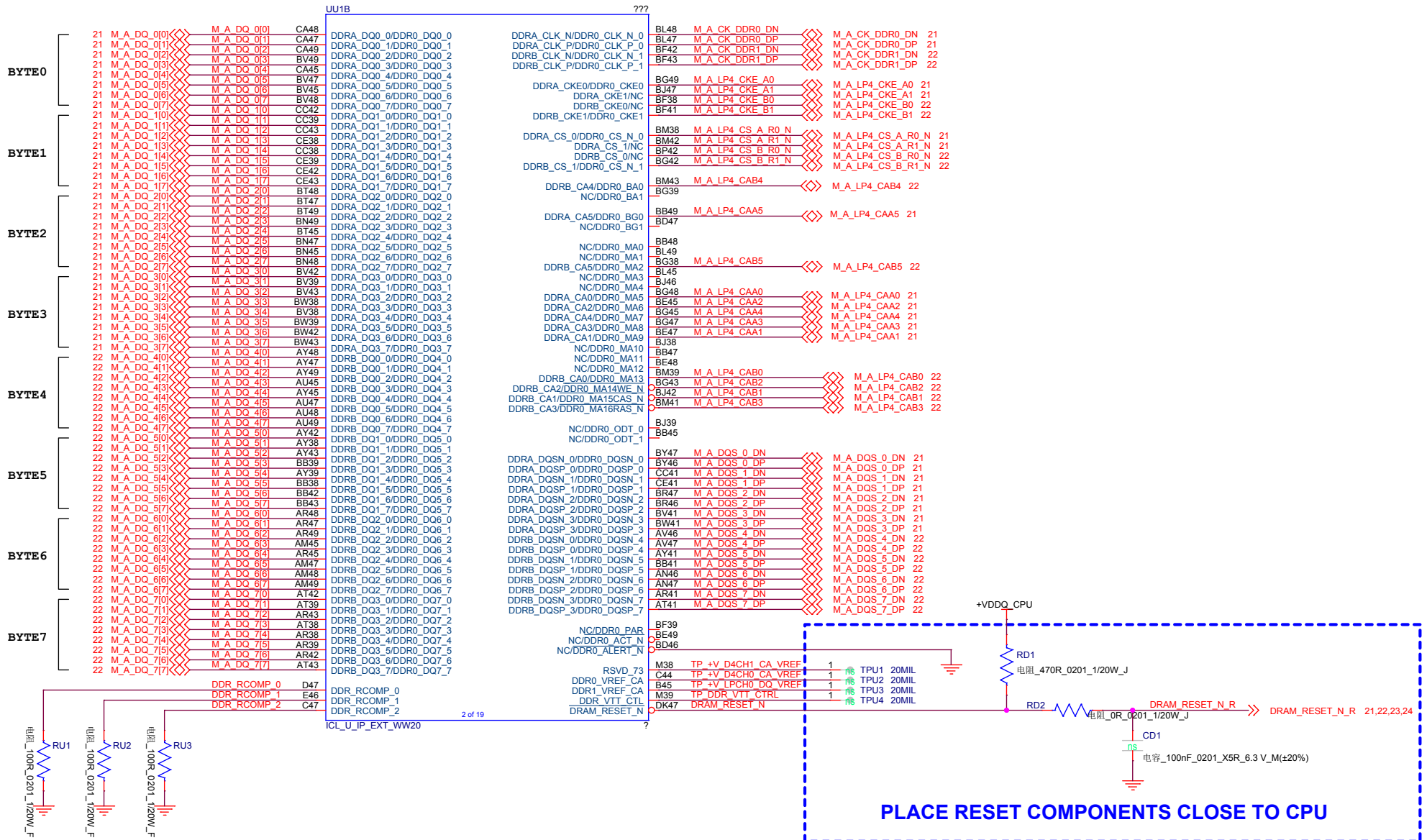
### KB BL ID

| HW_ID6 | Description           |
|--------|-----------------------|
| 0      | No keyboard Backlight |
| 1      | Keyboard Backlight    |

### Reserve ID

| HW_ID7 | Description |
|--------|-------------|
| 0      | Reserve     |
| 1      | Reserve     |

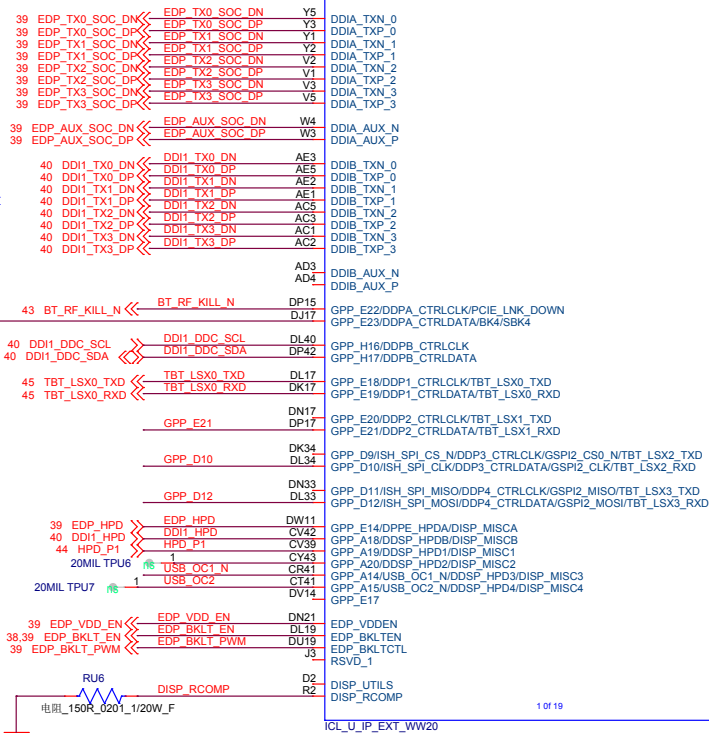






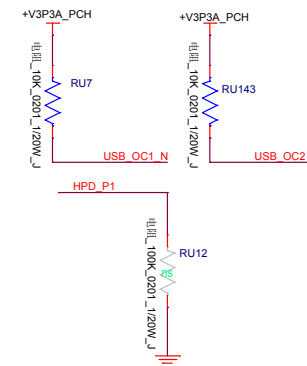
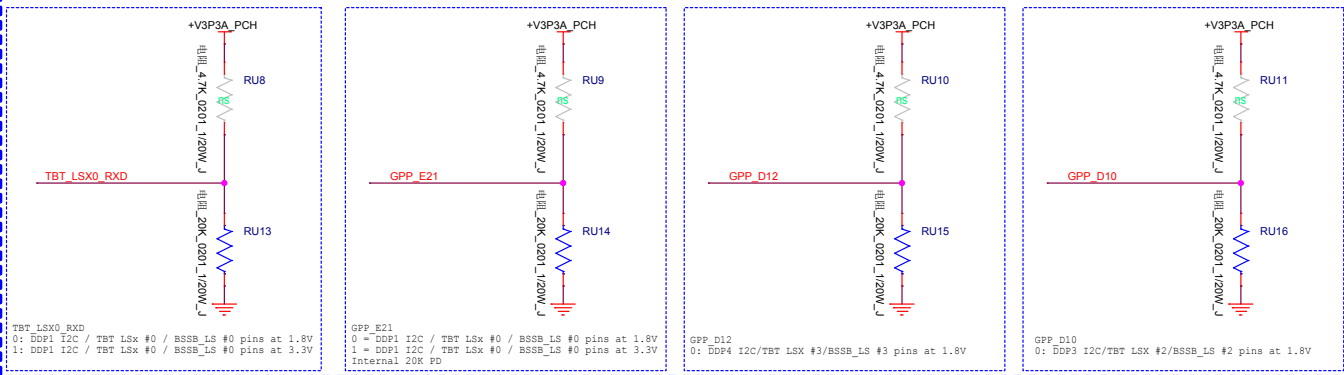
+V3P3A\_PCH

HDMI

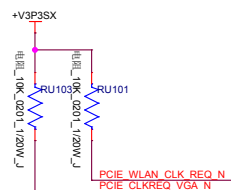
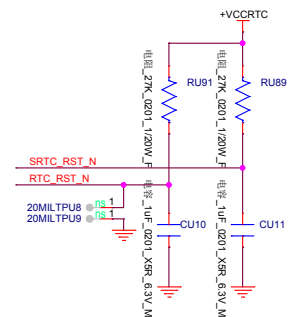
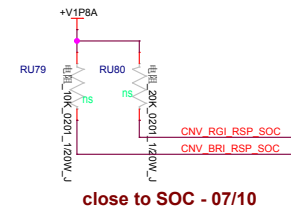
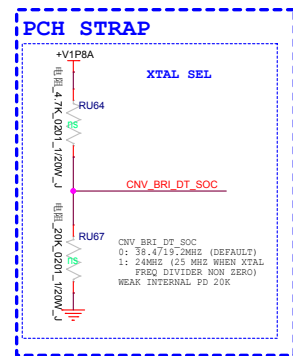


1 of 19

## PCH STRAP---VCCIO CONFIGURATION

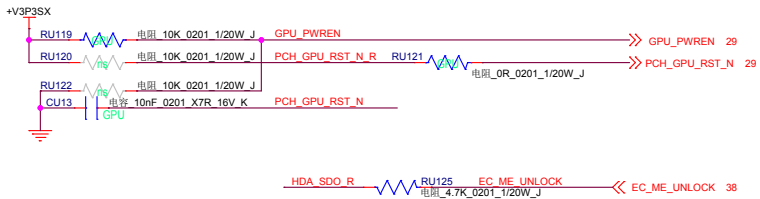




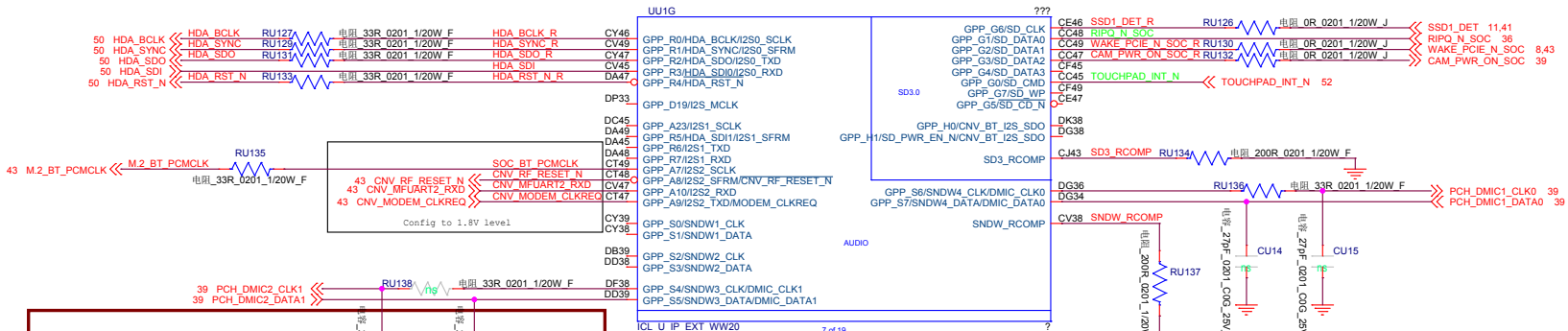




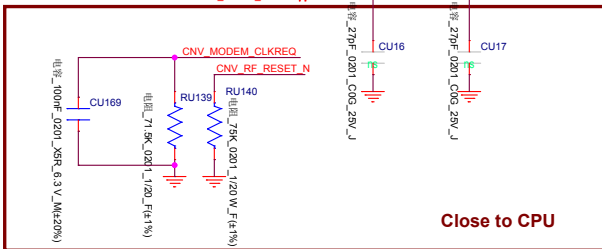
12.44 I2C\_PD\_SDC\_INT\_N >> I2C\_PD\_SDC\_INT\_N RU218 电阻 0R\_0201\_1/20W\_J GPPC\_B23\_SML1\_ALERT\_N



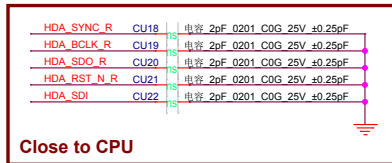
HDA\_SDO\_R 电阻 4.7K\_0201\_1/20W\_J EC\_ME\_UNLOCK 38



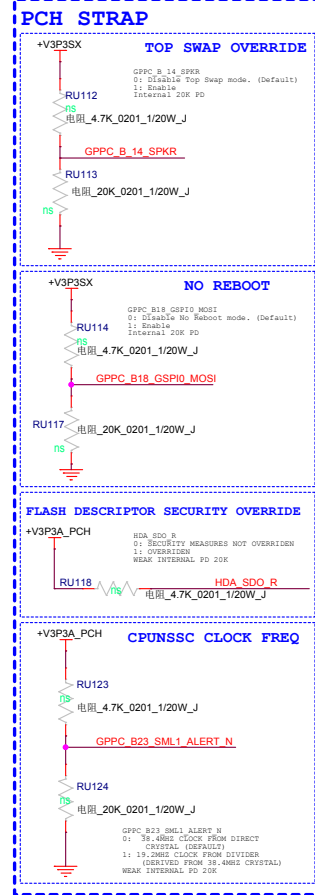
39 PCH\_DMIC2\_CLK1 39 PCH\_DMIC2\_DATA1



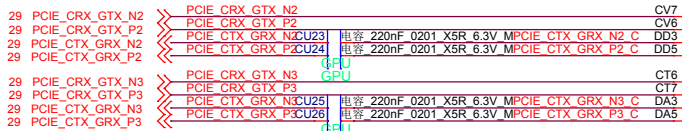
Close to CPU



Close to CPU

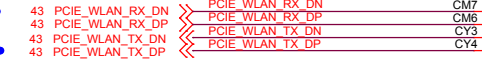


GPU

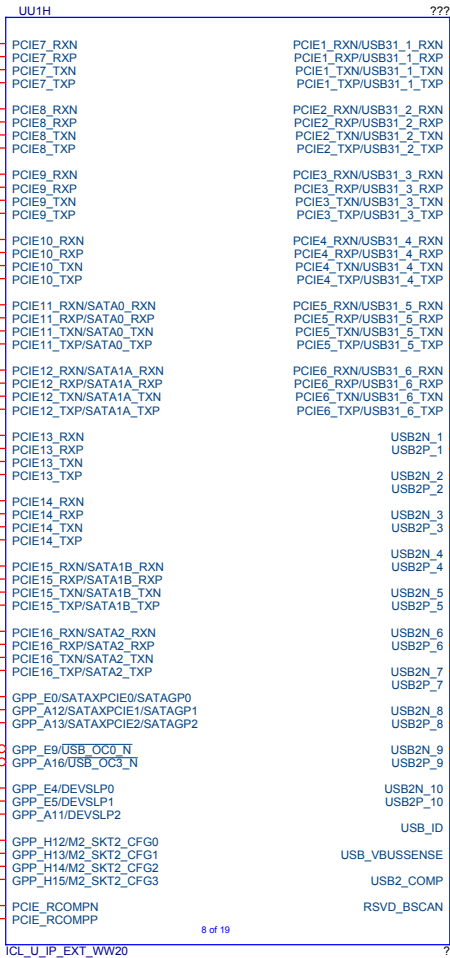
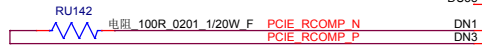
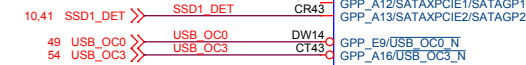
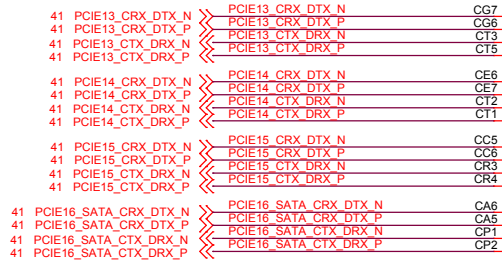


NA

WLAN



SSD1



8 of 19

USB3.0 TypeA 1 AUO

NA

NA

NA

GPU

USB3.0 Type-A 1 AUO

NA

Type-C

DB USB2.0 Type-A

Finger Print

Camera

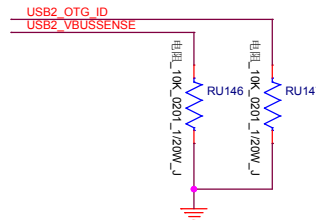
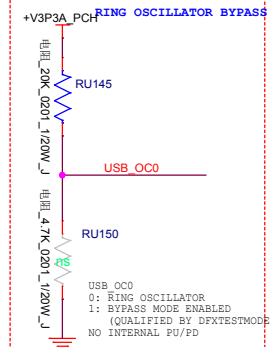
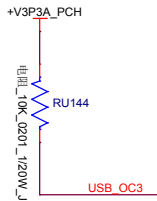
NA

NA

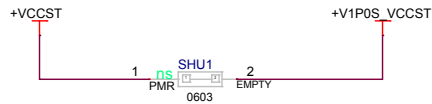
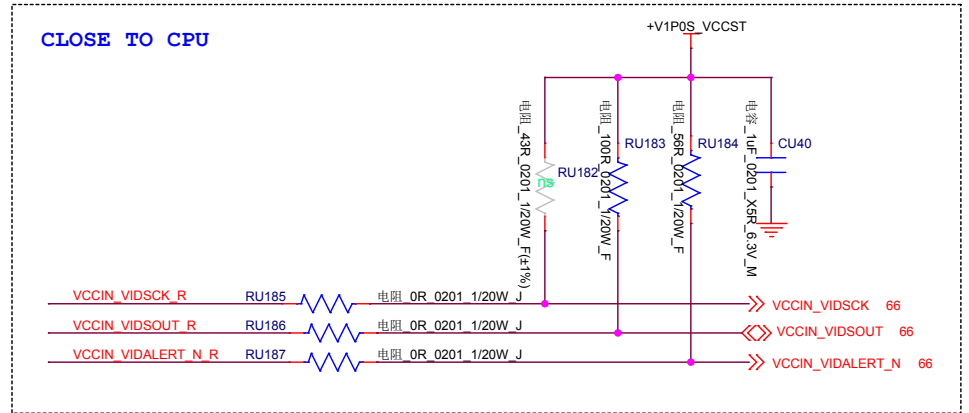
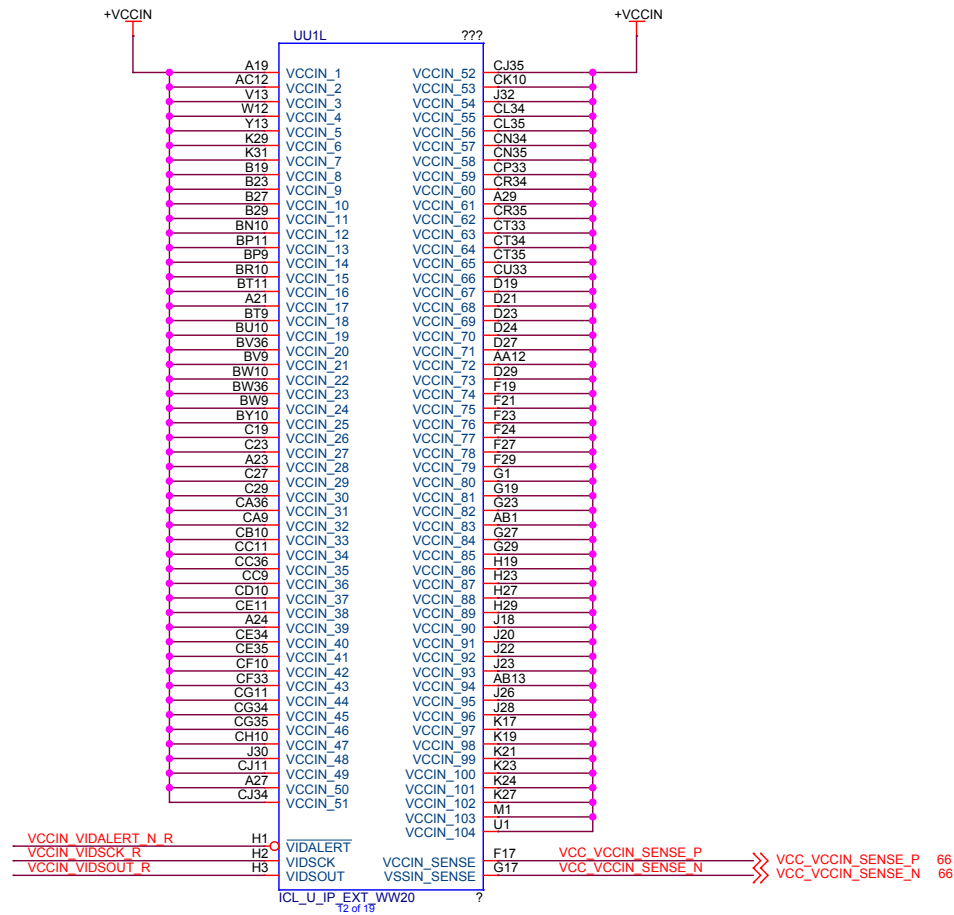
Touch Panel

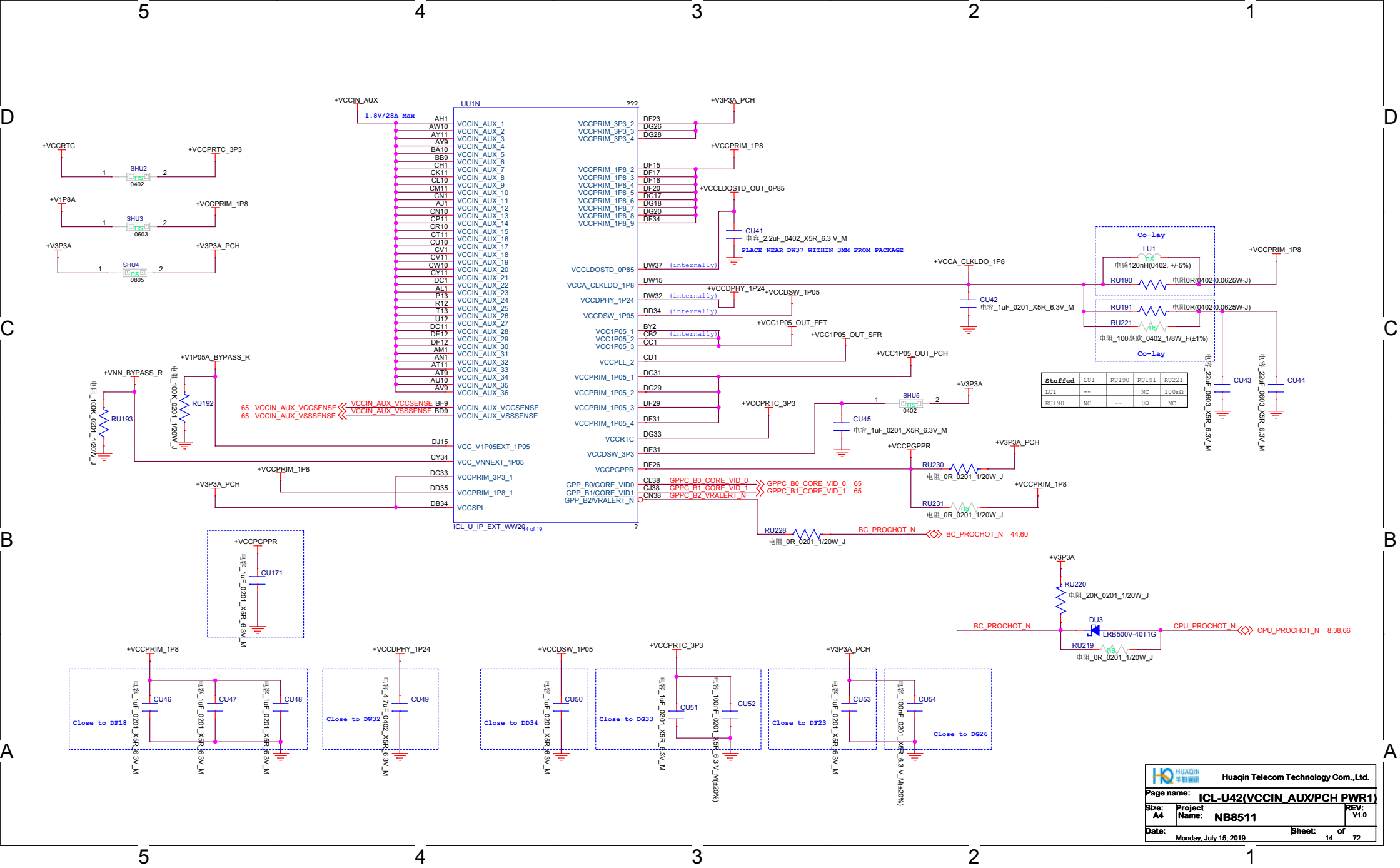
BT

## PCH STRAP

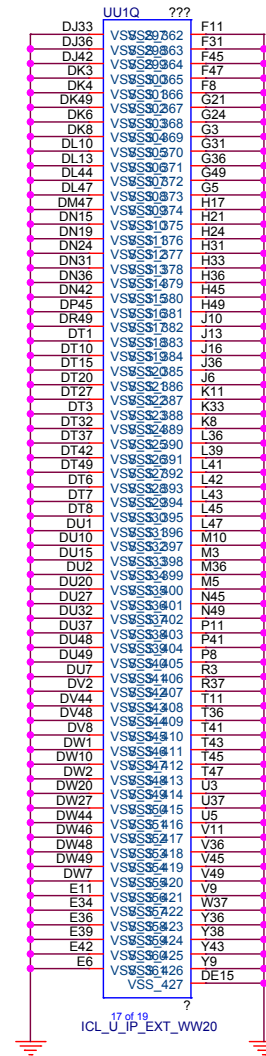
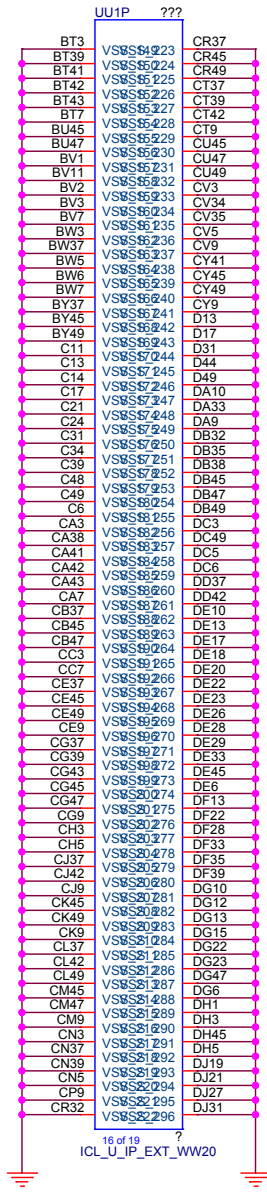
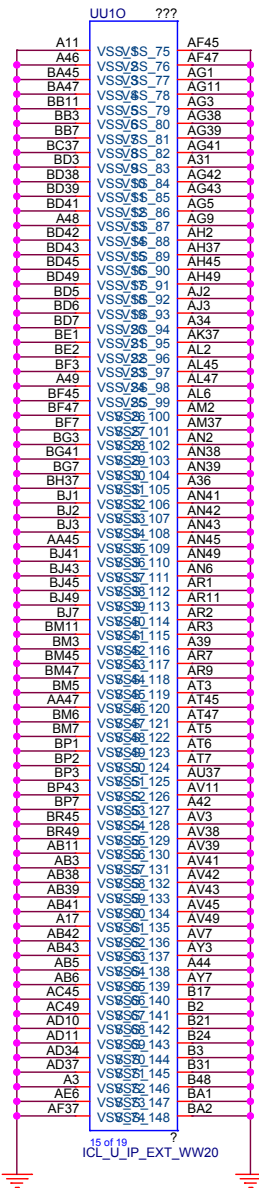


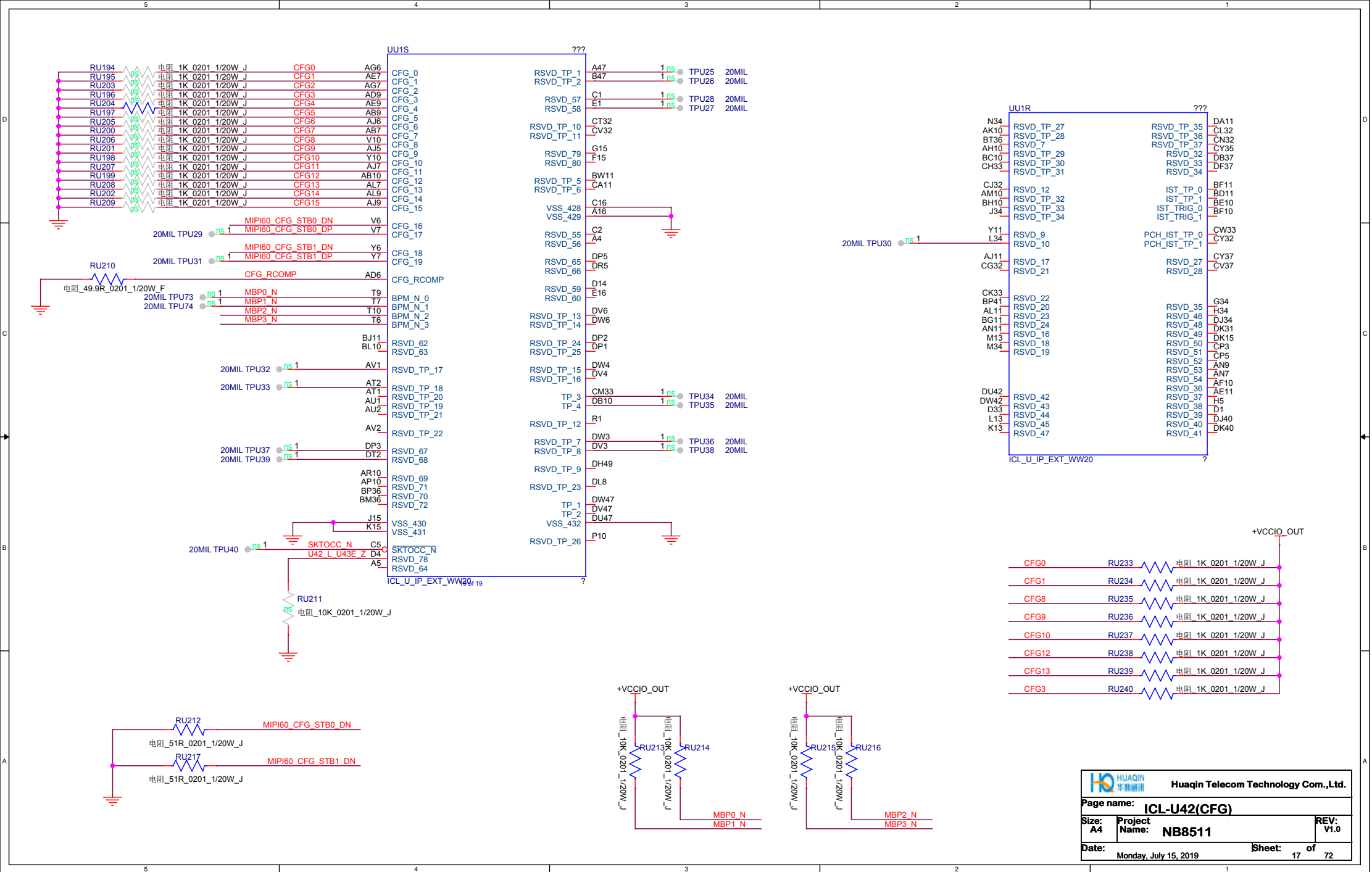


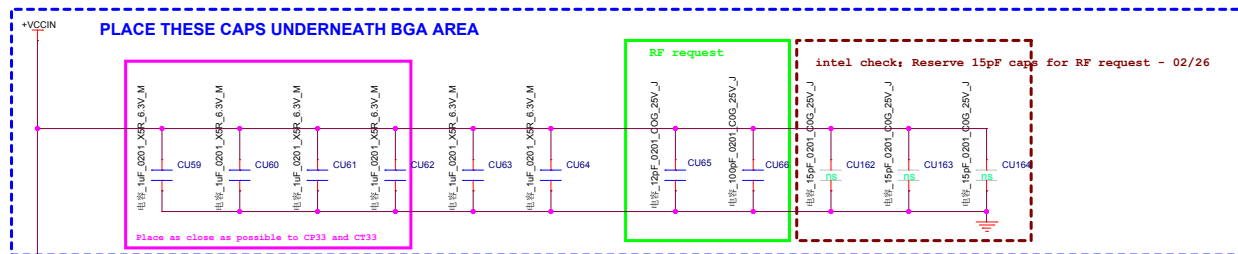






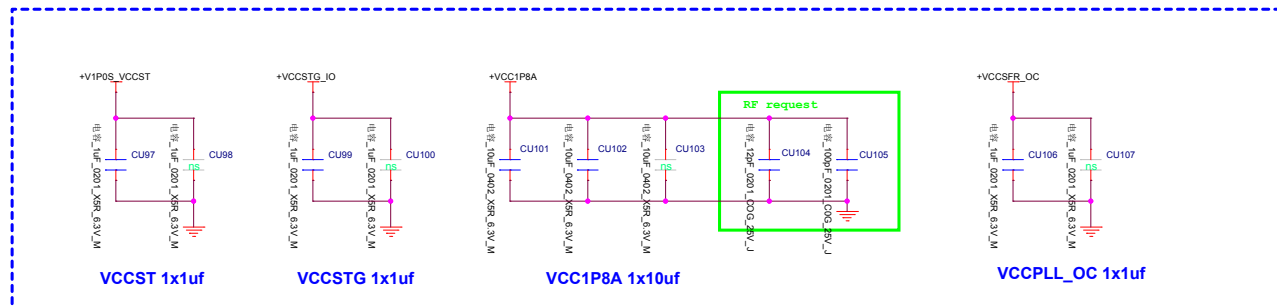
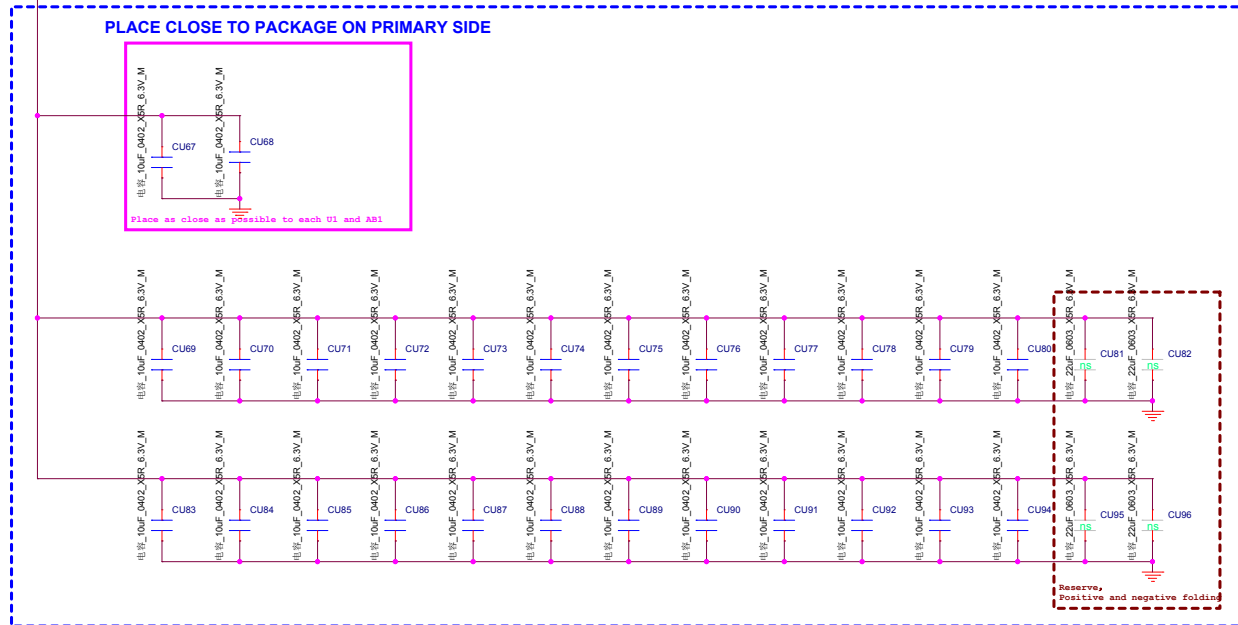


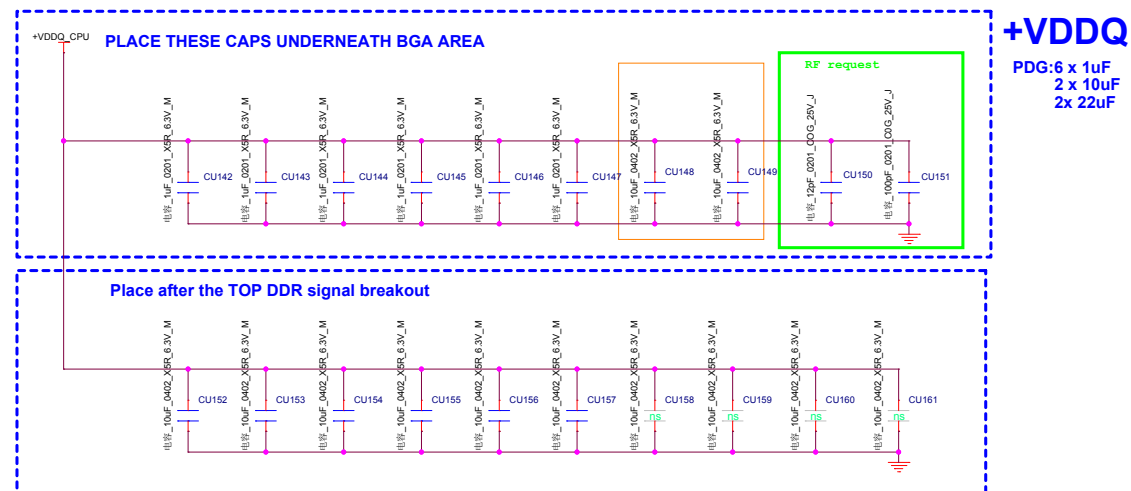
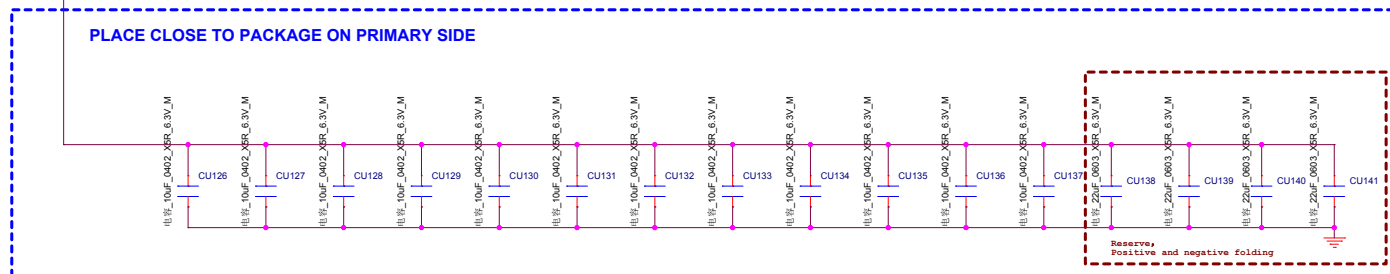
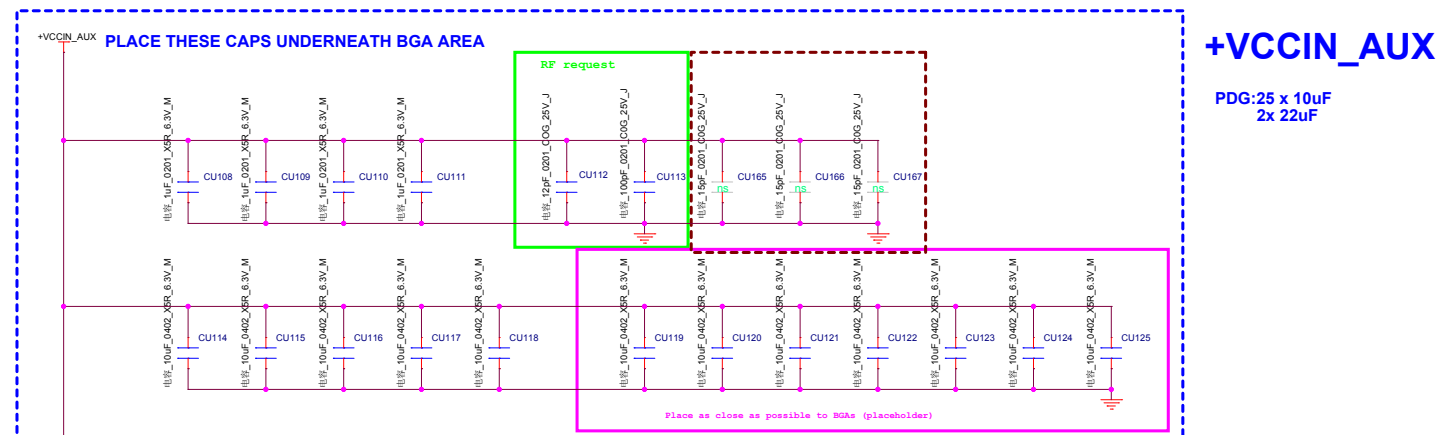




**+VCCIN**

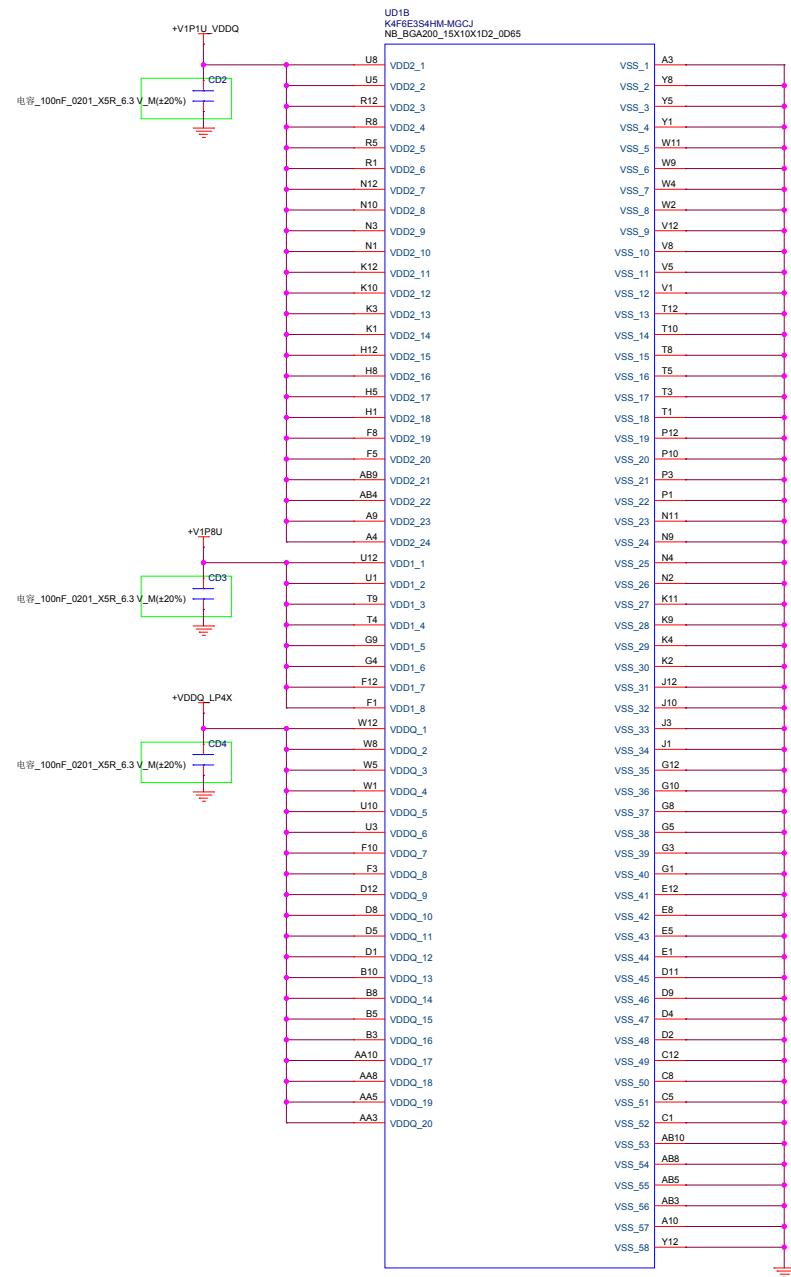
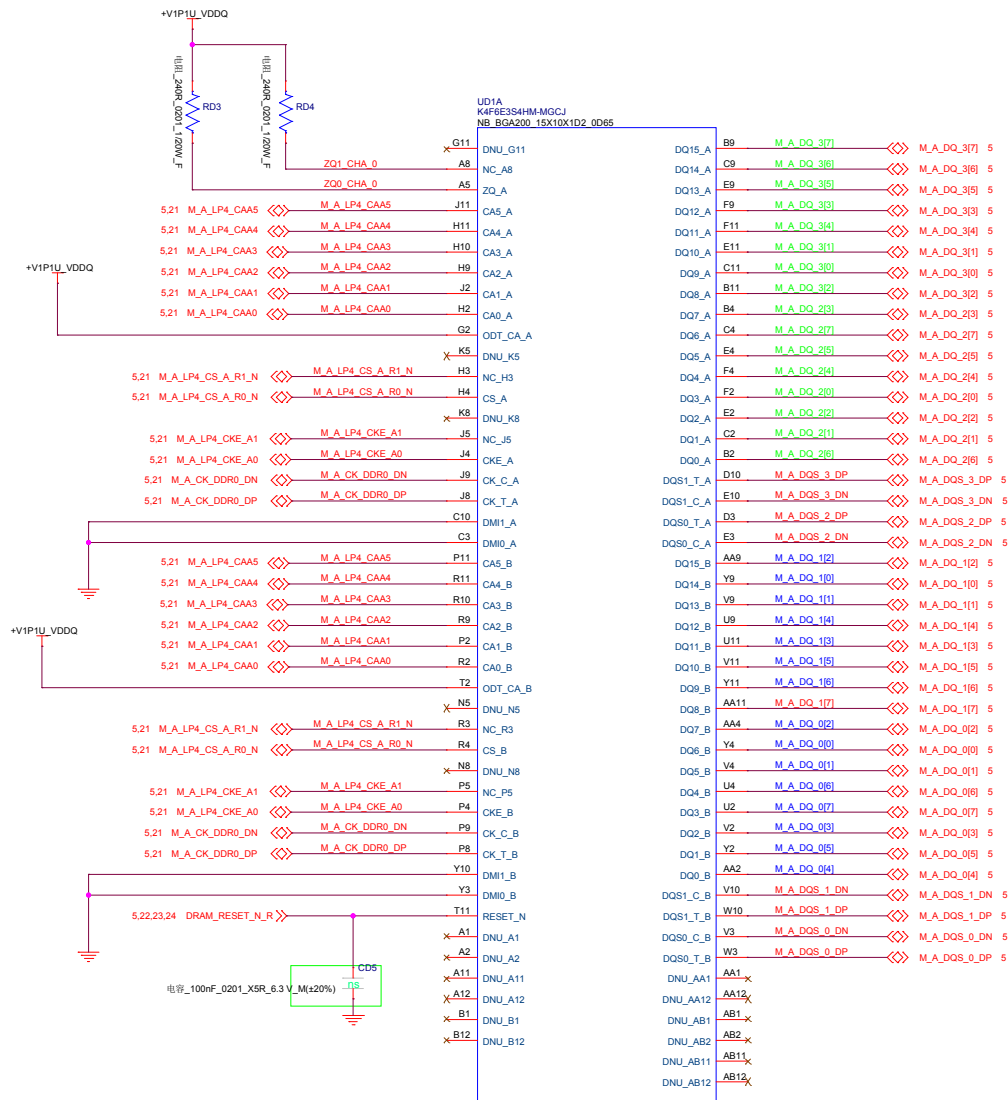
PDG:4 x 1uF  
2 x 10uF  
10x 22uF  
3x 47uF

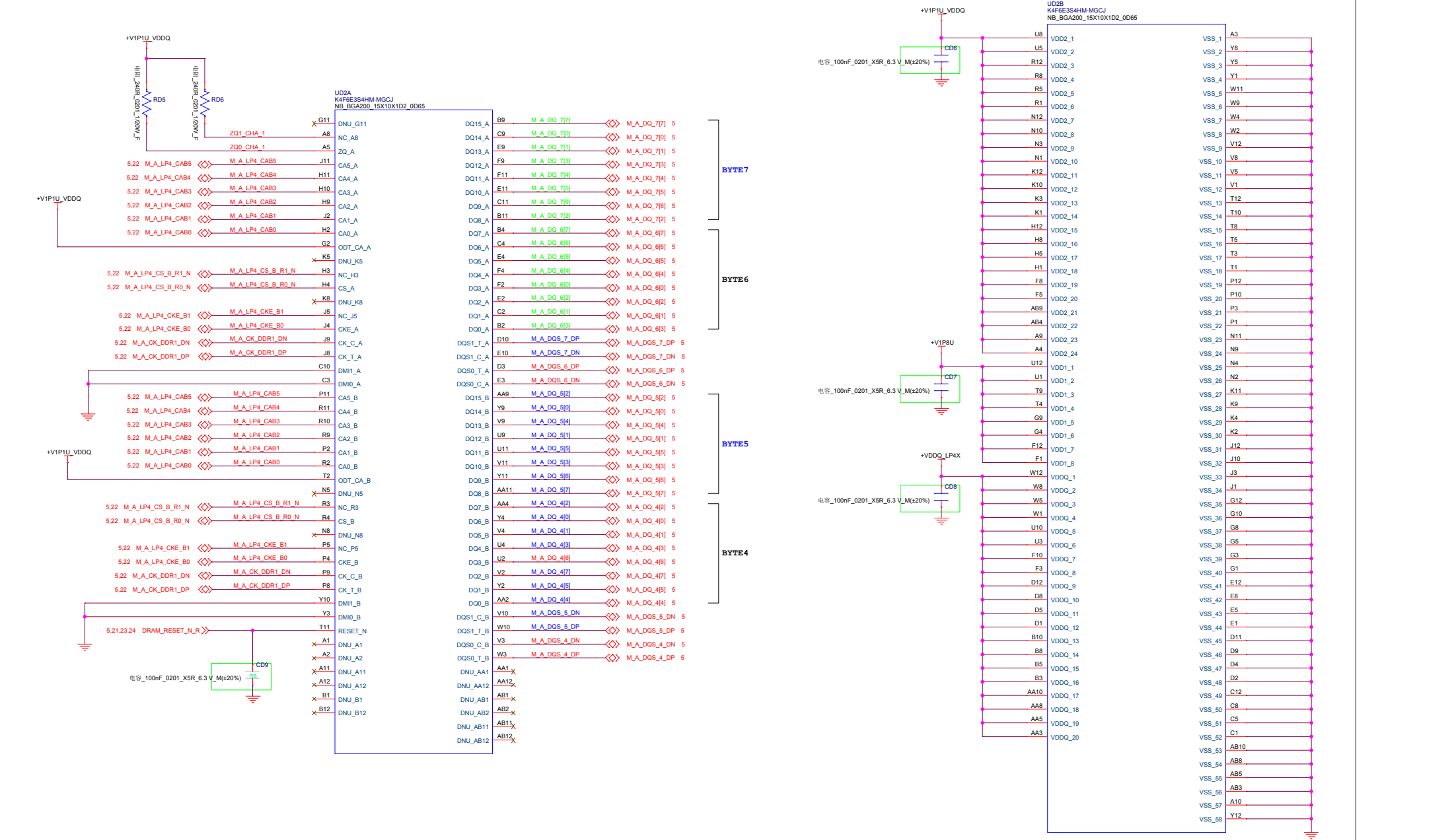


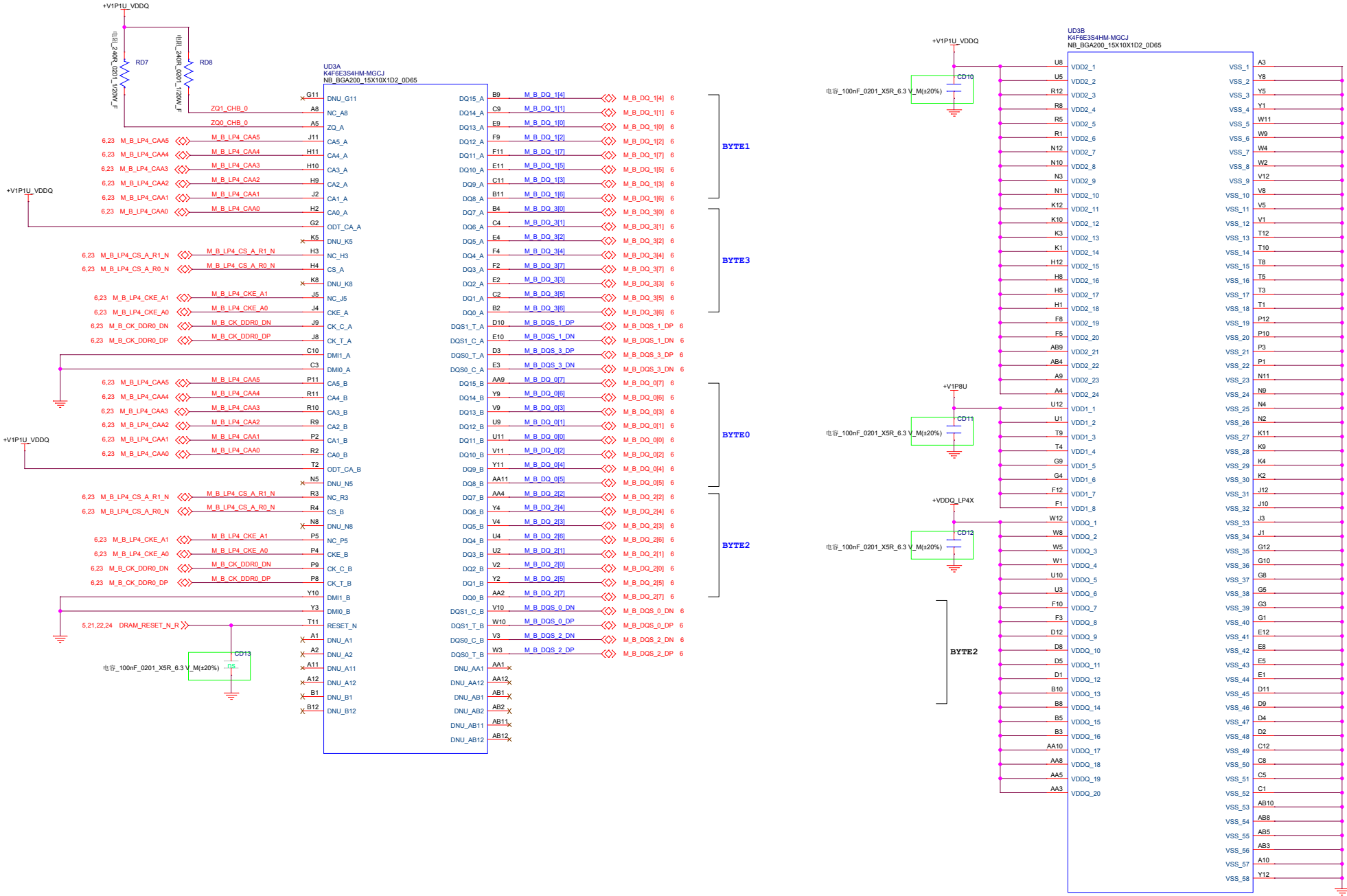


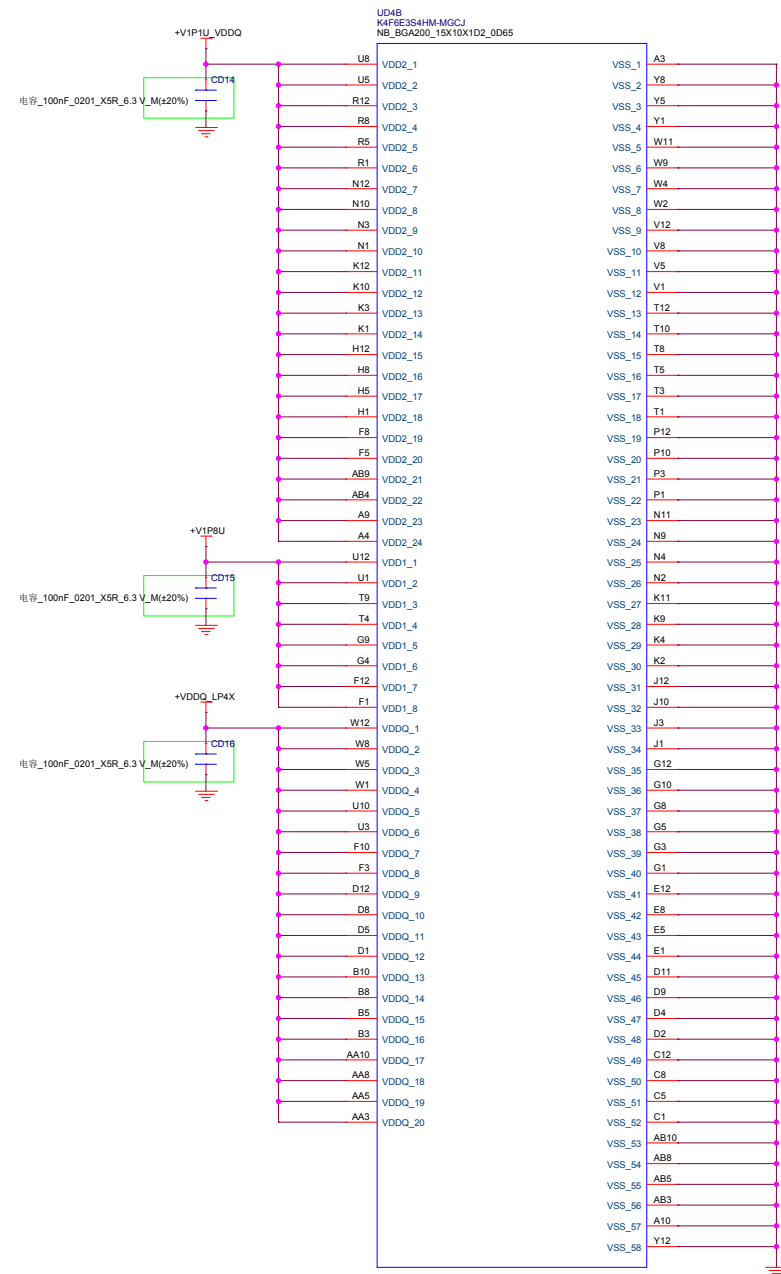
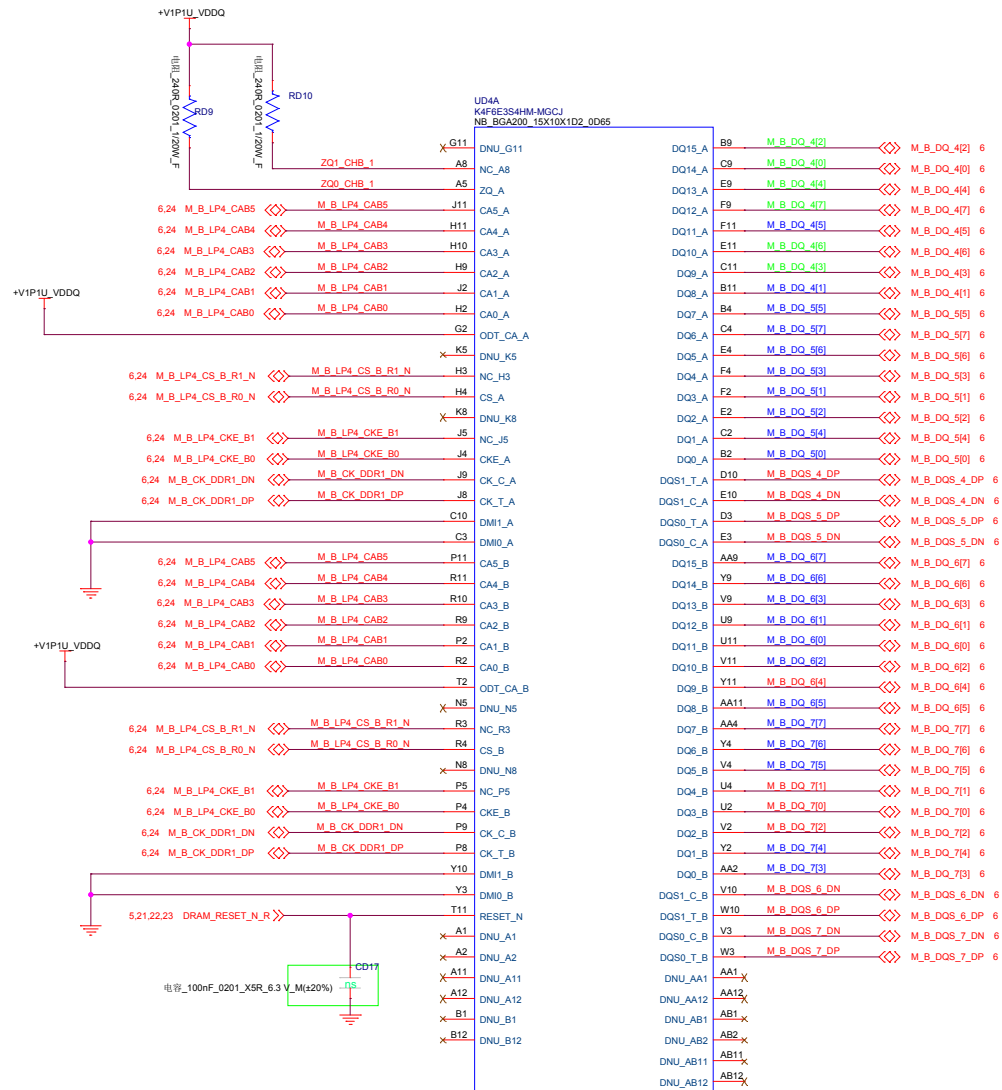


# CHA-1



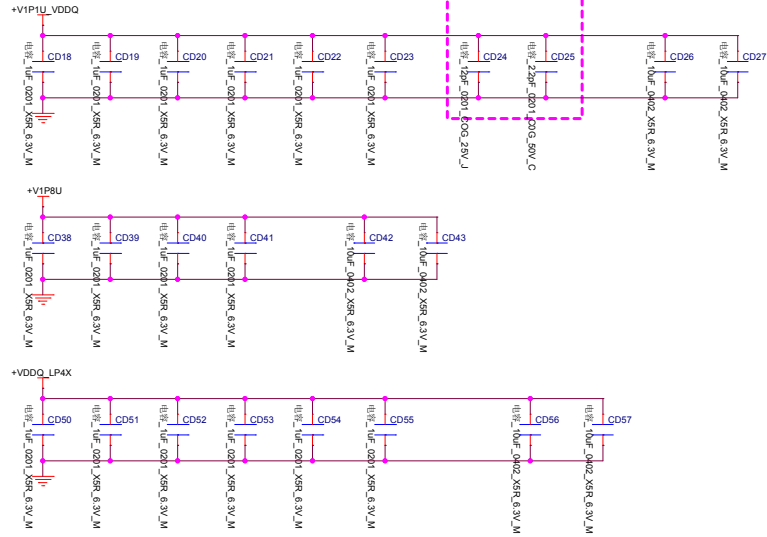




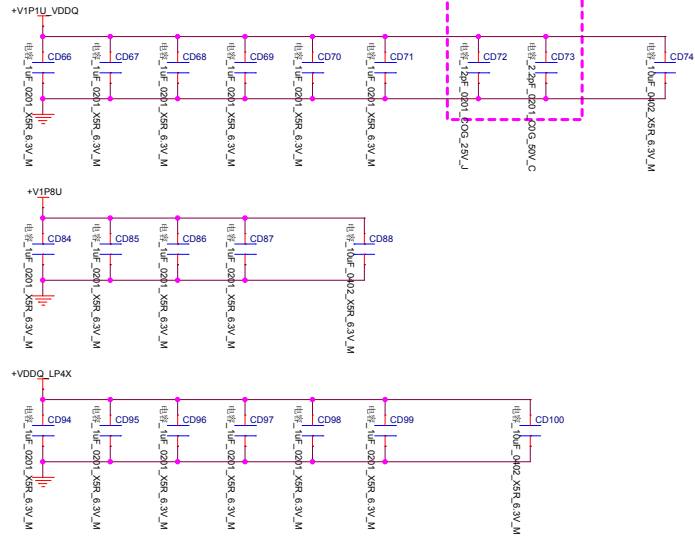


## DECOUPLING CAPACITORS FOR LPDDR4 CHANNEL A

Place as close as possible to UD?

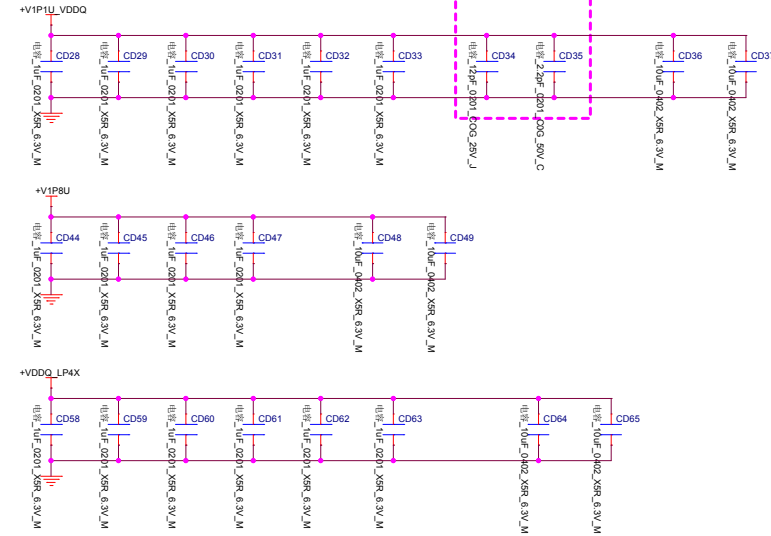


Place as close as possible to UD?

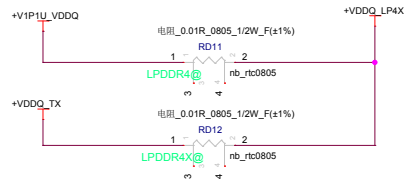
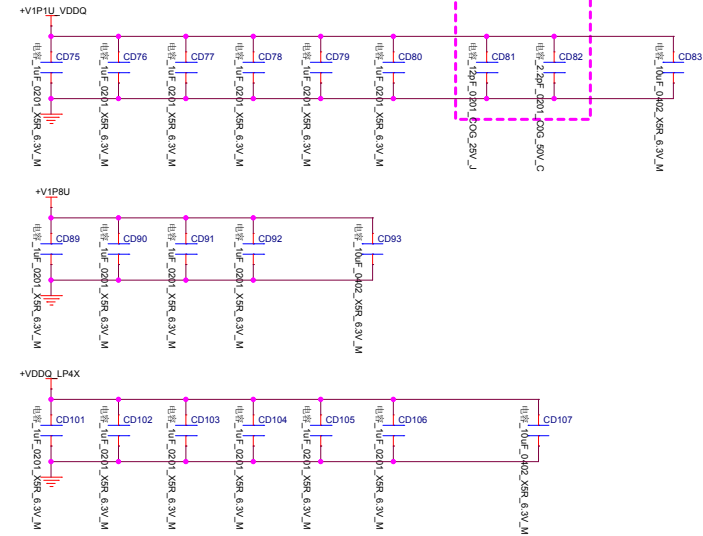


## DECOUPLING CAPACITORS FOR LPDDR4 CHANNEL B

Place as close as possible to UD?



Place as close as possible to UD?



|   |   |   |   |   |
|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 |
| D |   |   |   | D |
| C |   |   |   | C |
| B |   |   |   | B |
| A |   |   |   | A |
| 5 | 4 | 3 | 2 | 1 |

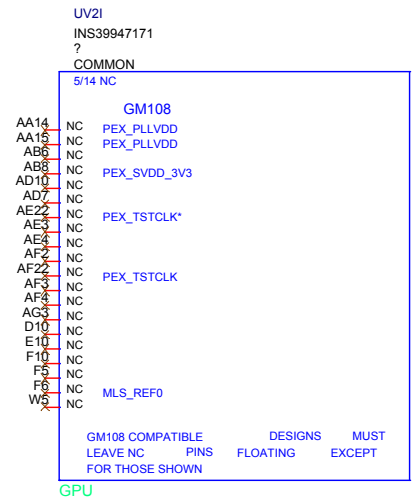
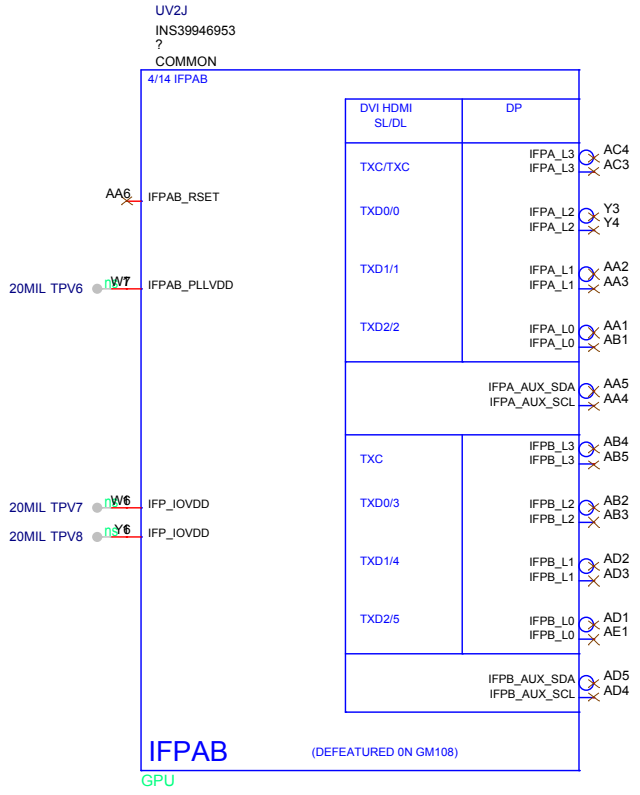
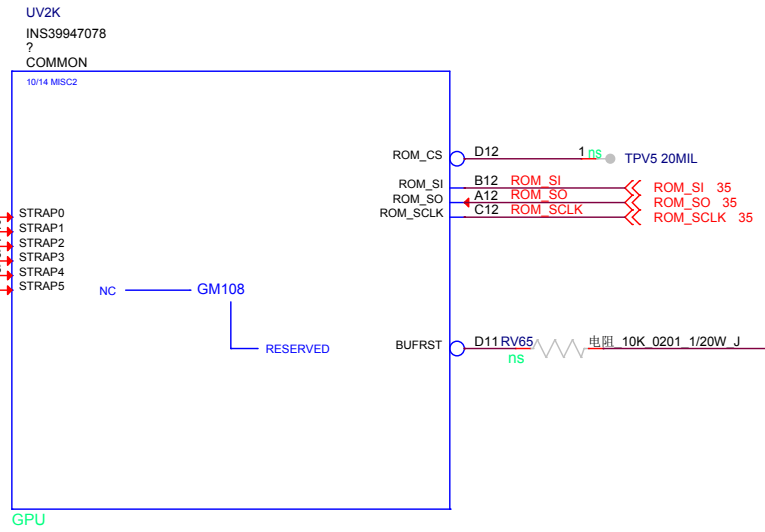
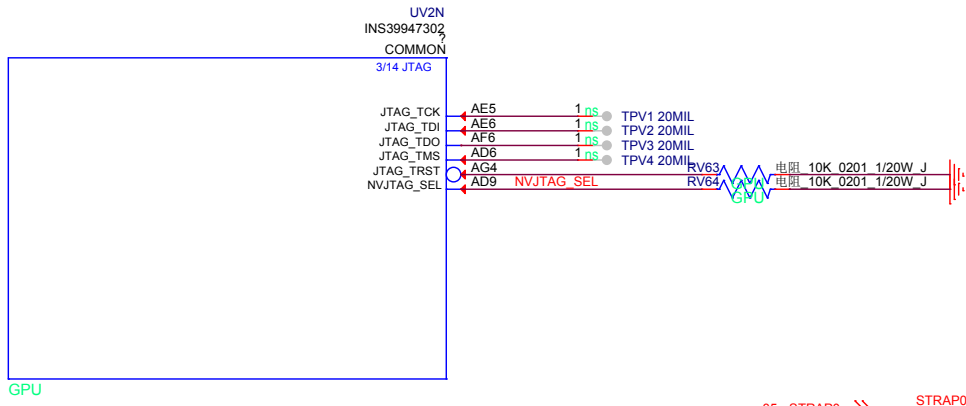
|                                                                                       |  |                             |  |                                     |                  |
|---------------------------------------------------------------------------------------|--|-----------------------------|--|-------------------------------------|------------------|
|  |  | HUAQIN<br>华勤通讯              |  | Huaqin Telecom Technology Com.,Ltd. |                  |
| Page name: <b>BLANK</b>                                                               |  |                             |  |                                     |                  |
| Size: <b>A4</b>                                                                       |  | Project Name: <b>NB8511</b> |  |                                     | REV: <b>V1.0</b> |
| Date: <b>Monday, July 15, 2019</b>                                                    |  |                             |  | Sheet: <b>26</b>                    | of <b>72</b>     |

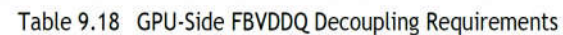
|   |   |   |   |   |   |
|---|---|---|---|---|---|
|   | 5 | 4 | 3 | 2 | 1 |
| D |   |   |   |   |   |
| C |   |   |   |   |   |
| B |   |   |   |   |   |
| A |   |   |   |   |   |
|   | 5 | 4 | 3 | 2 | 1 |

|                                                                                       |  |                                |  |                                     |              |
|---------------------------------------------------------------------------------------|--|--------------------------------|--|-------------------------------------|--------------|
|  |  | HUAQIN<br>华勤通讯                 |  | Huaqin Telecom Technology Com.,Ltd. |              |
| Page name: <b>BLANK</b>                                                               |  |                                |  |                                     |              |
| Size:<br>A4                                                                           |  | Project<br>Name: <b>NB8511</b> |  |                                     | REV:<br>V1.0 |
| Date: <b>Monday, July 15, 2019</b>                                                    |  |                                |  | Sheet: <b>27</b> of <b>72</b>       |              |



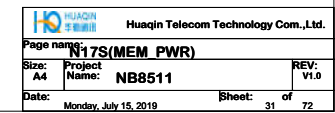






| FBVDDQ Decoupling Requirements                                                |          |                                                                 |
|-------------------------------------------------------------------------------|----------|-----------------------------------------------------------------|
| Recommended Quantity and Placement<br>(for all supported partitions combined) |          |                                                                 |
| Size                                                                          | Quantity | Placement                                                       |
| <b>2C-64 (preliminary)</b>                                                    |          |                                                                 |
| 6S [0402]                                                                     | 8        | Under GPU FBVDDQ ball (evenly distributed throughout partition) |
| 6S [0603]                                                                     | 2        |                                                                 |
| 6S [0603]                                                                     | 1        | Near GPU device                                                 |
| 6S [0603]                                                                     | 3        |                                                                 |
| <b>4C-128 (preliminary)</b>                                                   |          |                                                                 |
| 6S [0402]                                                                     | 12       | Under GPU FBVDDQ ball (equally distributed across partitions)   |
| 6S [0603]                                                                     | 4        |                                                                 |
| 6S [0603]                                                                     | 2        | Near GPU device                                                 |
| 6S [0603]                                                                     | 5        |                                                                 |
| <b>B4-256</b>                                                                 |          |                                                                 |
| 6S [0402]                                                                     | 24       | Under GPU FBVDDQ ball (equally distributed across partitions)   |
| 6S [0603]                                                                     | 5        |                                                                 |
| 6S [0603]                                                                     | 7        | Near GPU device                                                 |
| 6S [0603]                                                                     | 9        |                                                                 |

**Move to Power Page 2018/06/07**





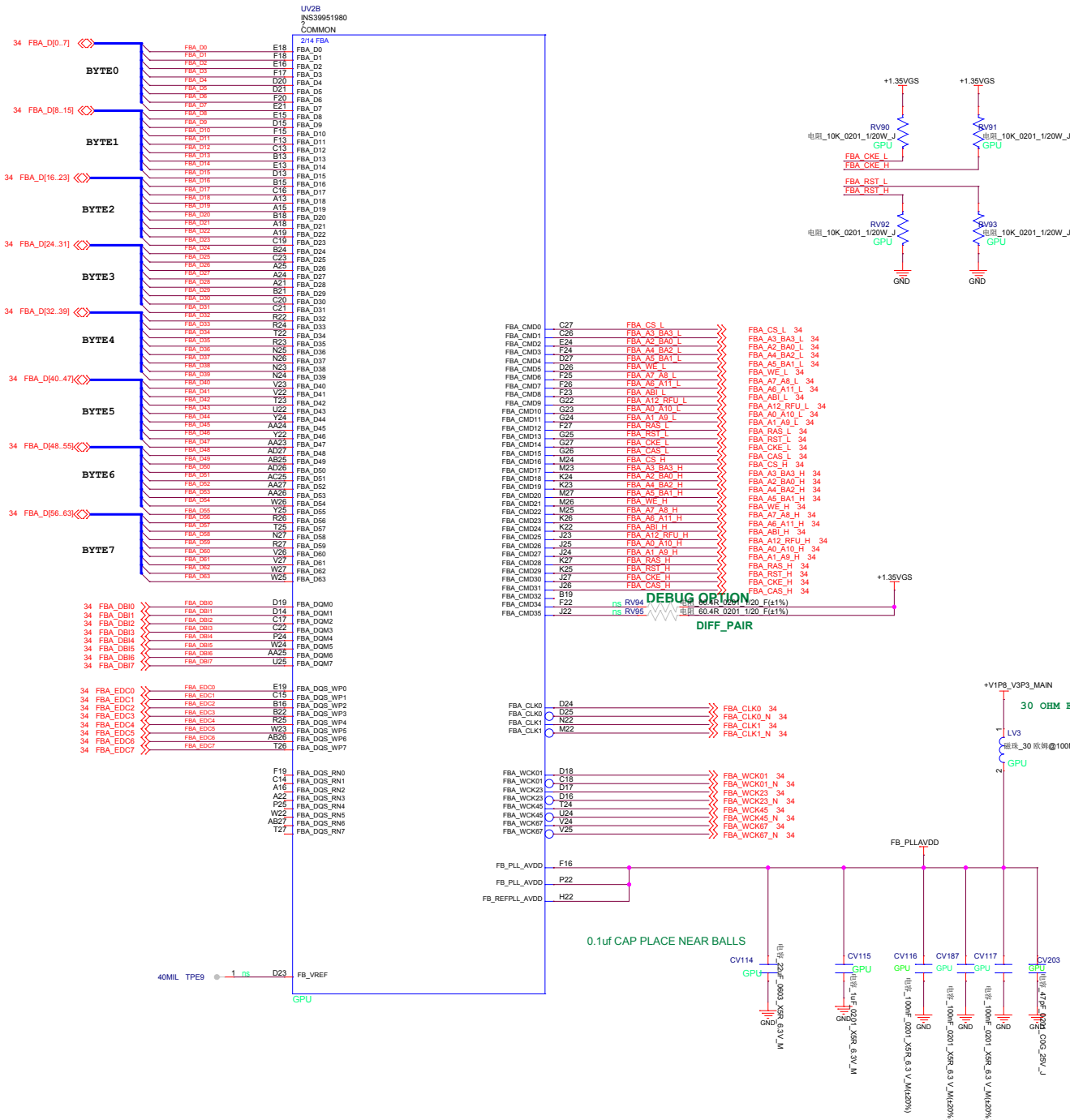


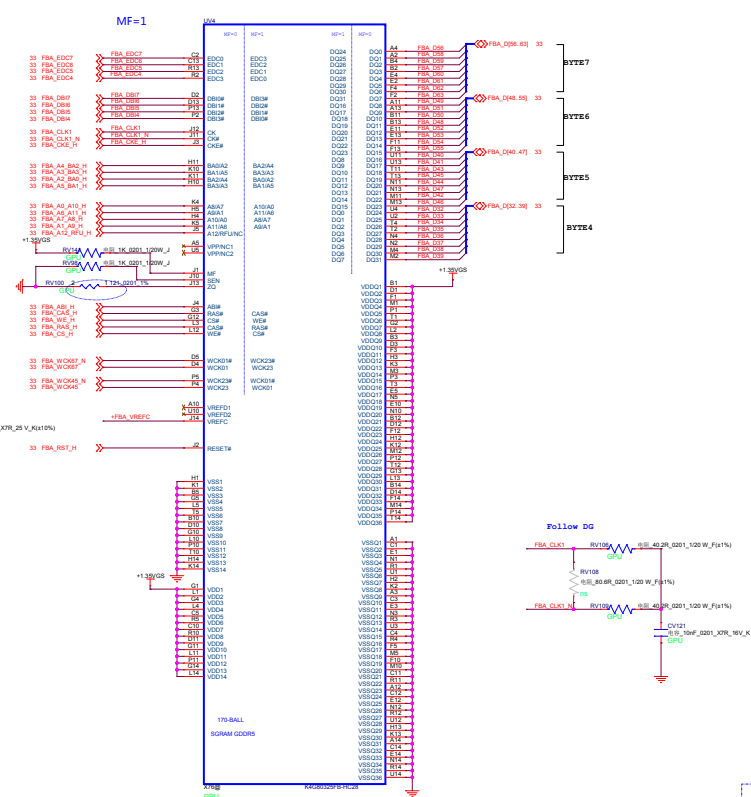
Table 7-4. GDDR5 Mode H Mapping

| GB2-64, GB28-64, GB48-128               | Channel 0 0..31     | GB2-64, GB28-64, GB48-128 | Channel 1 32..63 |
|-----------------------------------------|---------------------|---------------------------|------------------|
| CMD0                                    | CS*                 | CMD16                     | CS*              |
| CMD1                                    | A3_BA3              | CMD17                     | A3_BA3           |
| CMD2                                    | A2_BA0              | CMD18                     | A2_BA0           |
| CMD3                                    | A4_BA2              | CMD19                     | A4_BA2           |
| CMD4                                    | A5_BA1              | CMD20                     | A5_BA1           |
| CMD5                                    | WE*                 | CMD21                     | WE*              |
| CMD6                                    | A7_A8               | CMD22                     | A7_A8            |
| CMD7                                    | A6_A11              | CMD23                     | A6_A11           |
| CMD8                                    | AB1*                | CMD24                     | AB1*             |
| CMD9                                    | A12_RFU             | CMD25                     | A12_RFU          |
| CMD10                                   | A0_A10              | CMD26                     | A0_A10           |
| CMD11                                   | A1_A9               | CMD27                     | A1_A9            |
| CMD12                                   | RAS*                | CMD28                     | RAS*             |
| CMD13                                   | RST*                | CMD29                     | RST*             |
| CMD14                                   | CKE*                | CMD30                     | CKE*             |
| CMD15                                   | CAS*                | CMD31                     | CAS*             |
| GB2-64, GB28-64, GB48-128 Channel 0 & 1 |                     |                           |                  |
| CMD32                                   | Not used            |                           |                  |
| CMD33 <sup>1</sup>                      | Not used            |                           |                  |
| CMD34                                   | DEBUG0 <sup>2</sup> |                           |                  |
| CMD35                                   | DEBUG1 <sup>2</sup> |                           |                  |

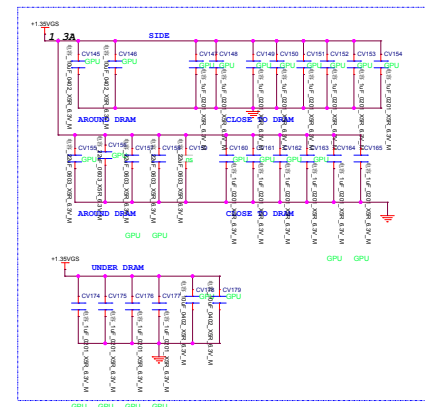
Notes:

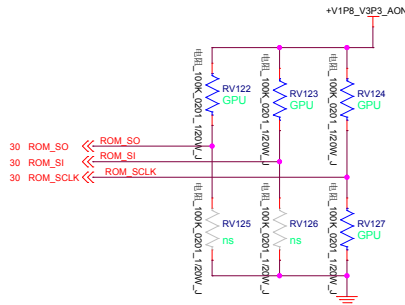
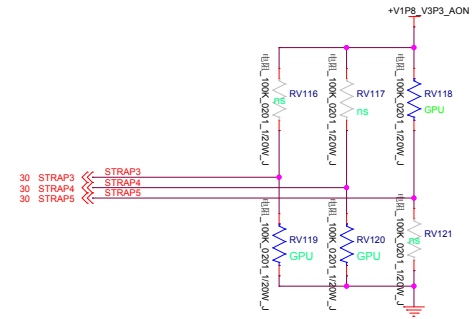
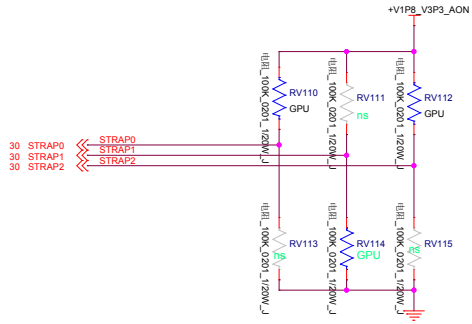
1. Not available in GB2-64 and GB28-64 packages.
2. GPU debug pins not connected to DRAM. See section 7.1.13.

## Memory - Upper 32 bits



Under GPO, RF require





For N17

| GPU        | Vendor  | Manufacturer       | Strap | Strap2 | Strap1 | Strap0 |
|------------|---------|--------------------|-------|--------|--------|--------|
| N17S-G1    | Samsung | K4G80325FB-HC28    | 0x0   | L      | L      | L      |
|            | Micron  | MT51J256M32HF-70:A | 0x1   | L      | L      | H      |
|            | Hynix   | H5GC8H24MJR-ROC    | 0x2   | L      | H      | L      |
|            | Micron  | MT51J256M32HF-70:B | 0x4   | H      | L      | L      |
| N17S_G0/G2 | Hynix   | H5GC8H24AJR-ROC    | 0x5   | H      | L      | H      |
|            | Micron  | MT51J256M32HF-80:B | 0x9   | L      | M      | L      |
|            | Hynix   | H5GC8H24AJR-R2C    | 0xA   | L      | M      | H      |

| PN           | MPN             | STRAP | Vendor  |
|--------------|-----------------|-------|---------|
| HQ1121499000 | K4G80325FB-HC28 | 0x00  | Samsung |
| HQ1121497000 | H5GC8H24MJR-R4C | 0x02  | Hynix   |

| Physical Strapping pin | Power Rail | RAM_CFG[3] | RAM_CFG[0x02] | RAM_CFG[1] | RAM_CFG[0x00] |
|------------------------|------------|------------|---------------|------------|---------------|
| STRAP0                 |            |            | L             |            | L             |
| STRAP1                 |            |            | H             |            | L             |
| STRAP2                 |            |            | L             |            | L             |
|                        |            |            |               |            |               |
|                        |            |            |               |            |               |
|                        |            |            |               |            |               |
|                        |            |            |               |            |               |

| SMBUS | ALT | ADDR                   |
|-------|-----|------------------------|
| 0     |     | 0x9E (Default)         |
| 1     |     | 0x9C (Multi-GPU usage) |

| DEVID | SEL       |
|-------|-----------|
| 0     | (Default) |
| 1     |           |

| PCIE | CFG       |
|------|-----------|
| 0    | (Default) |
| 1    |           |

| VGA | DEVICE                      |
|-----|-----------------------------|
| 0   | 3D Device (Class Code 302h) |
| 1   | VGA Device (Default)        |

| Physical Strapping pin | Power Rail | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
|------------------------|------------|--------------|--------------|--------------|--------------|
| ROM_SCLK               | M          |              |              |              |              |
| ROM_SI                 | H          | Disable      | Disable      | Disable      | Disable      |
| ROM_SO                 | H          |              |              |              |              |

Table 5.3 RAMCFG

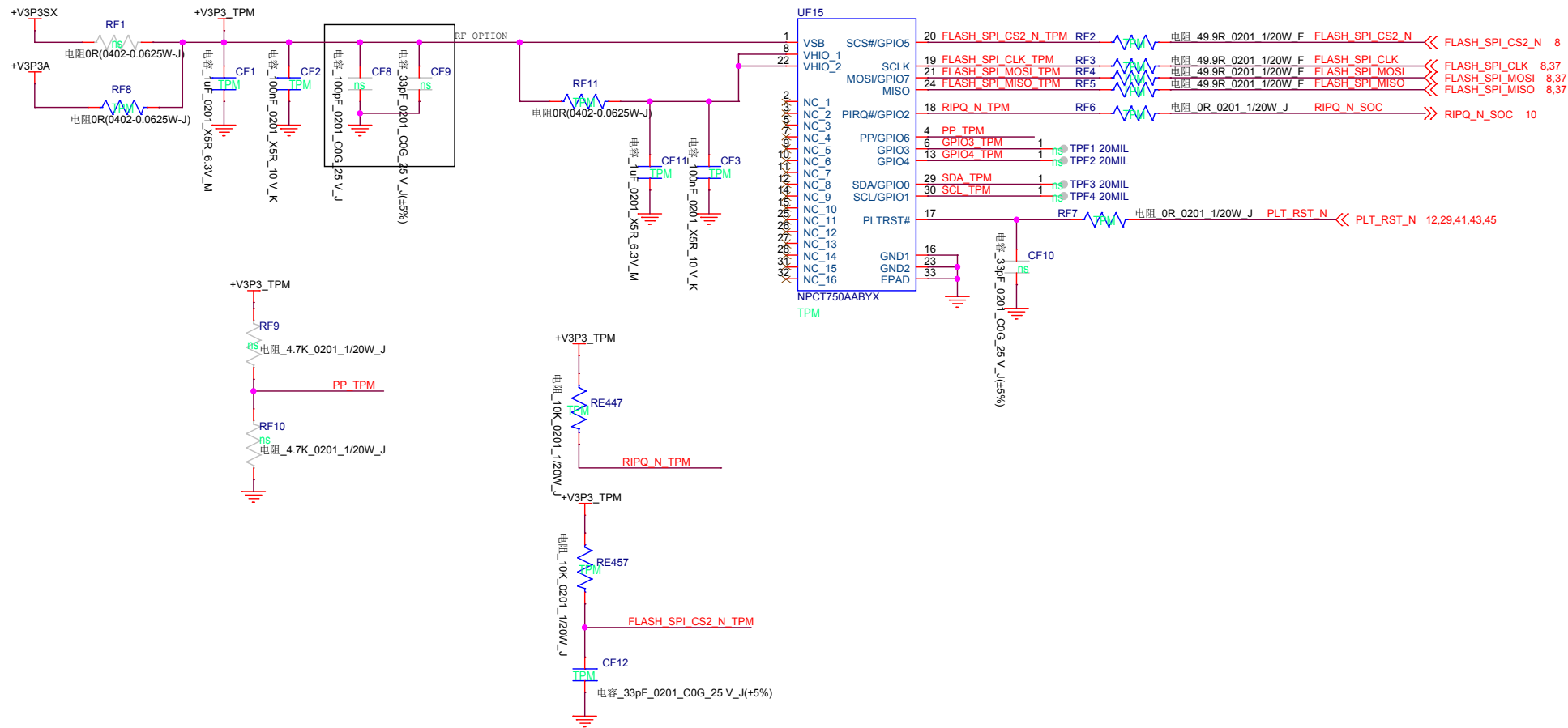
| Strap Pins <sup>see Note</sup> |        |        | RAMCFG Setting Number                                              |
|--------------------------------|--------|--------|--------------------------------------------------------------------|
| STRAP2                         | STRAP1 | STRAP0 | (see Memory RVL for memory configs corresponding to these numbers) |
| L                              | L      | L      | 0 (0x0000)                                                         |
| L                              | L      | H      | 1 (0x0001)                                                         |
| L                              | H      | L      | 2 (0x0002)                                                         |
| L                              | H      | H      | 3 (0x0003)                                                         |
| H                              | L      | L      | 4 (0x0004)                                                         |
| H                              | L      | H      | 5 (0x0005)                                                         |
| H                              | H      | L      | 6 (0x0006)                                                         |
| H                              | H      | H      | 7 (0x0007)                                                         |
| L                              | L      | M      | 8 (0x0008)                                                         |
| L                              | M      | L      | 9 (0x0009)                                                         |
| L                              | M      | H      | 10 (0x000A)                                                        |
| L                              | H      | M      | 11 (0x000B)                                                        |
| M                              | L      | L      | 12 (0x000C)                                                        |
| M                              | L      | H      | 13 (0x000D)                                                        |

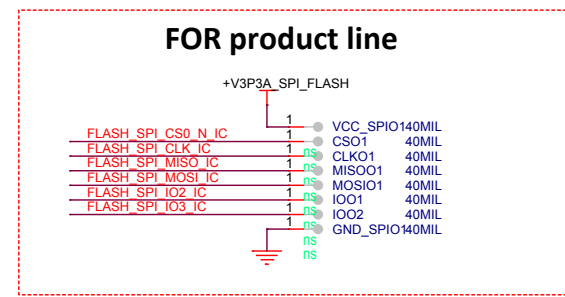
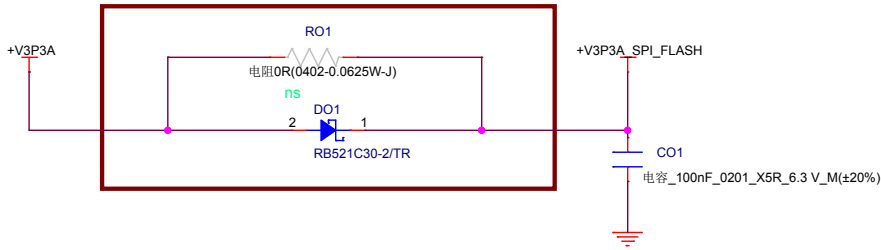
Table 5. N17S-G0/G2 GDDR5 Recommended Memories

| Memory Density | Allowed Memory Configuration | FBVDD/Q | Vendor | Manufacturer Part Number | Die Revision | Strap | Memory Speed Grade | Date Code Alert | Qual Plan | Status           |
|----------------|------------------------------|---------|--------|--------------------------|--------------|-------|--------------------|-----------------|-----------|------------------|
| 8 Gb           | 256Mx32 512Mx16              | 1.35V   | Micron | MT51J256M32HF-80:B       | B-die        | 0x9   | 8 Gbps             | N/A             | Full      | Production ready |
|                |                              |         | Hynix  | H5GC8H24AJR-R2C          | A-die        | 0xA   | 8 Gbps             | N/A             | Full      | Production ready |

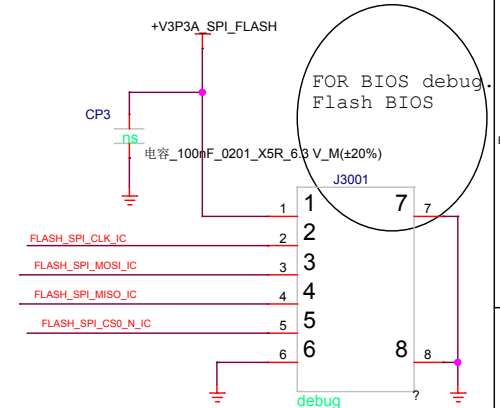
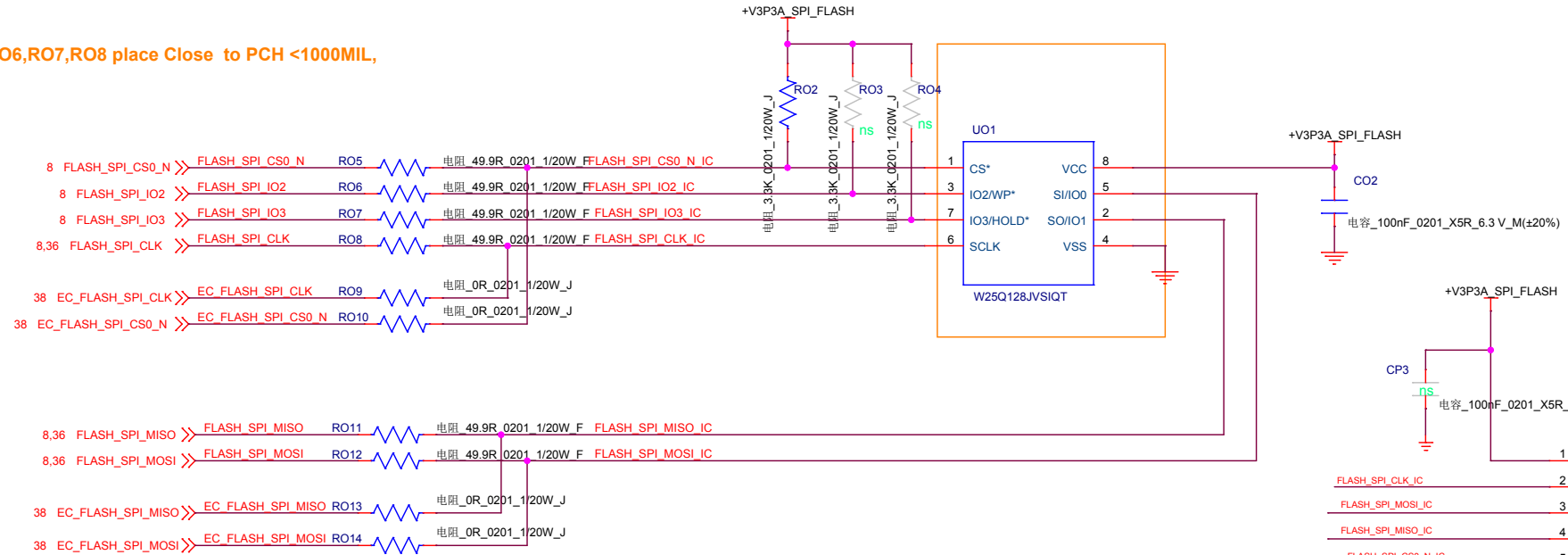
Notes:

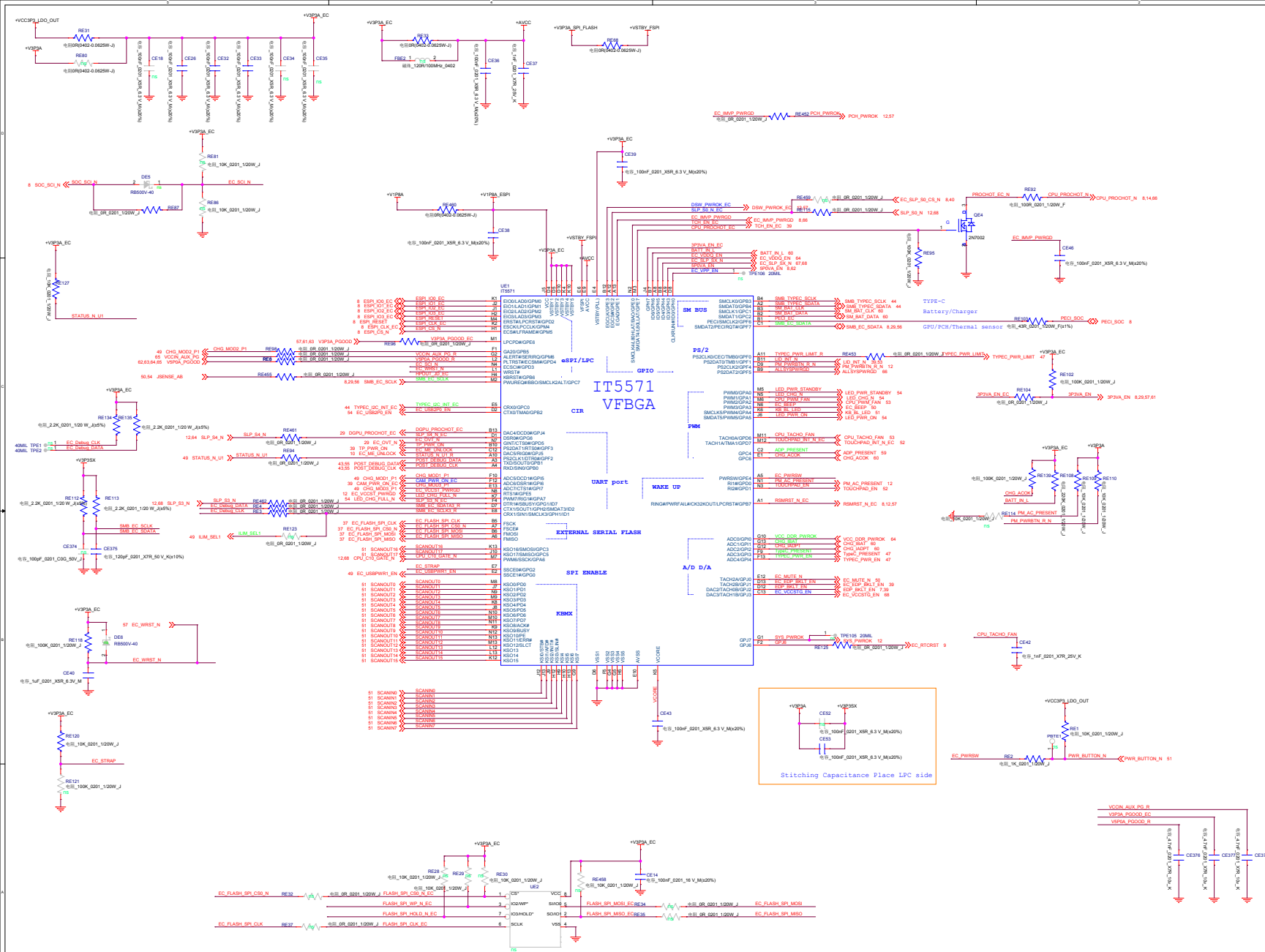
- For N17S-G0/G2, the maximum allowable memory case temperature is 85 °C.
- N17S-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations in Table 4 for N17S-G1.



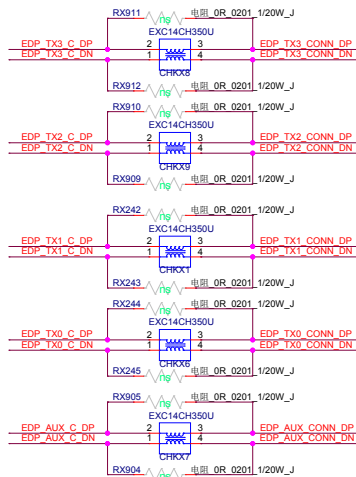
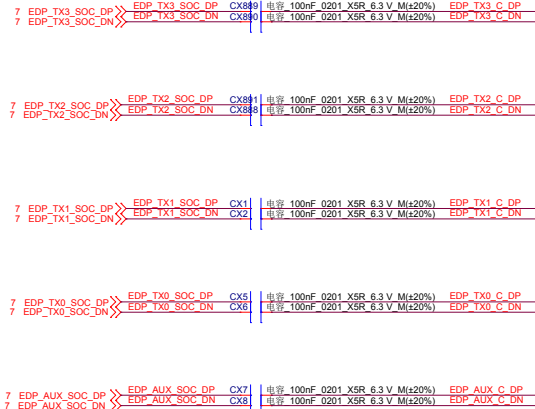


Series RO5,RO6,RO7,RO8 place Close to PCH <1000MIL,

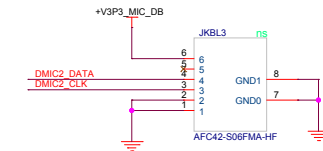
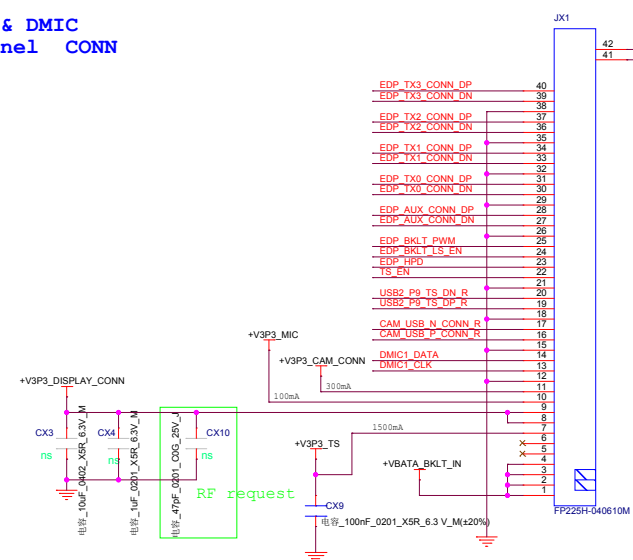




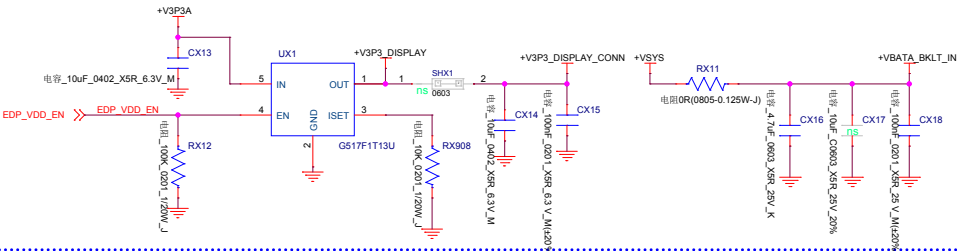
## eDP Signal



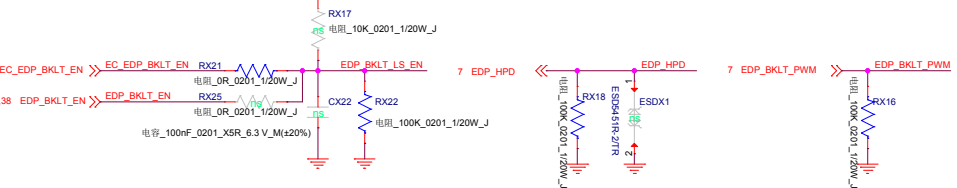
## eDP & CAM & DMIC & Touch Panel CONN



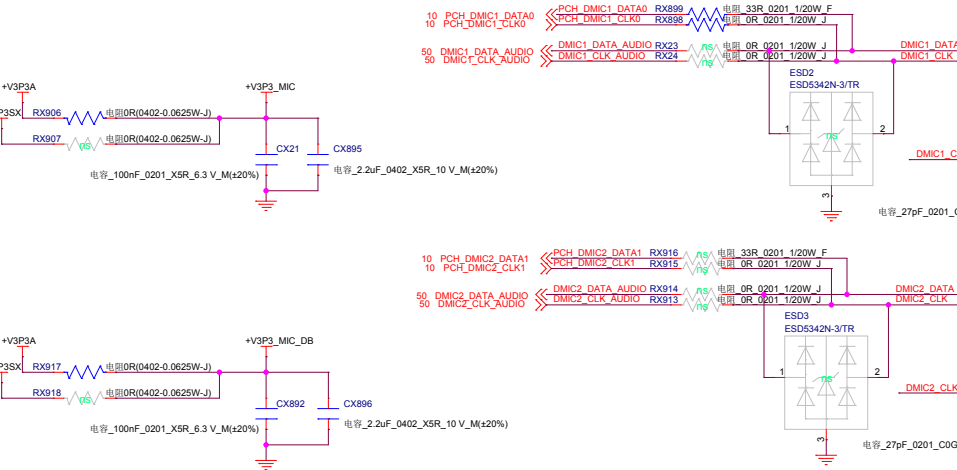
## eDP VCC & BL Power



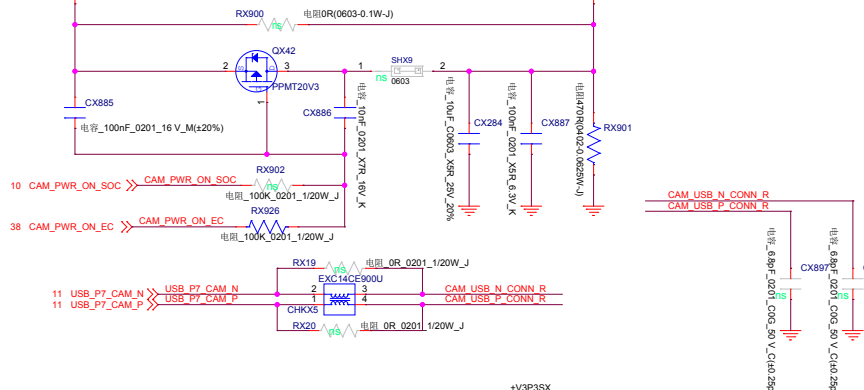
## eDP Control



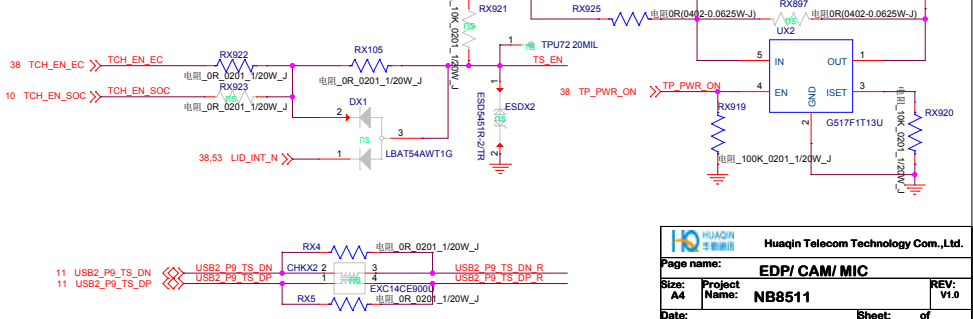
## MIC



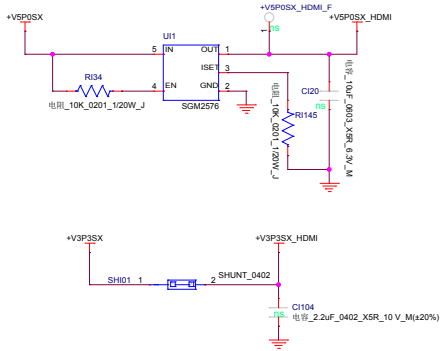
## CAM Power



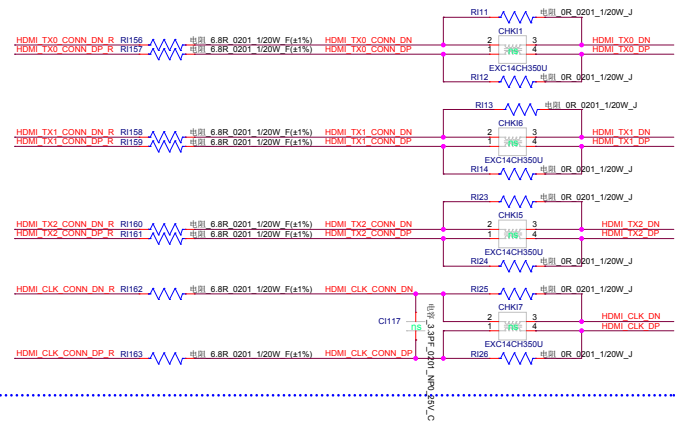
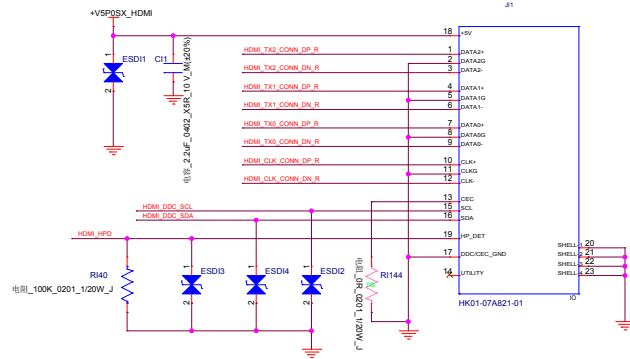
## Touch Panel



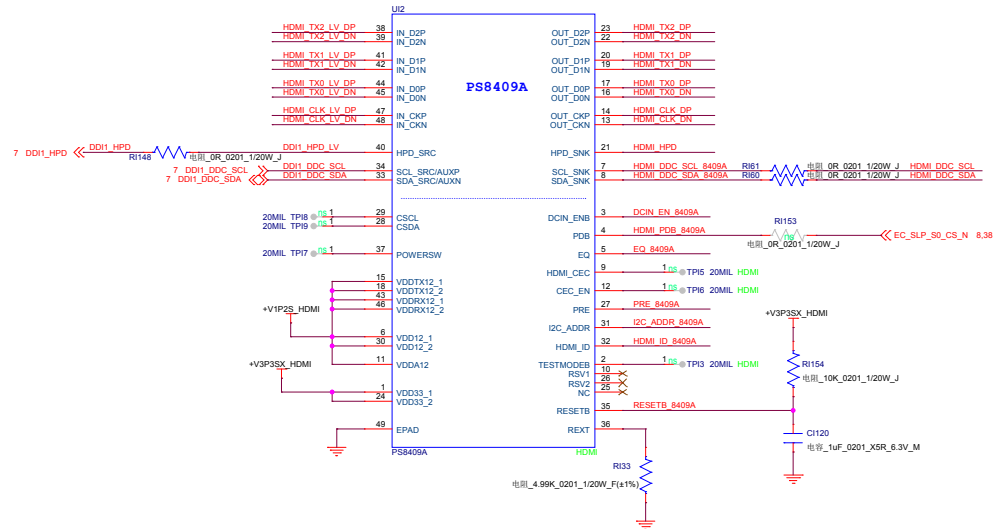
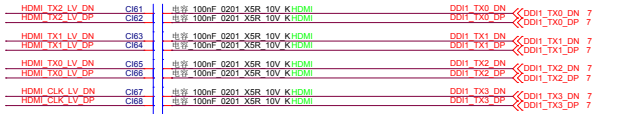
Power 1



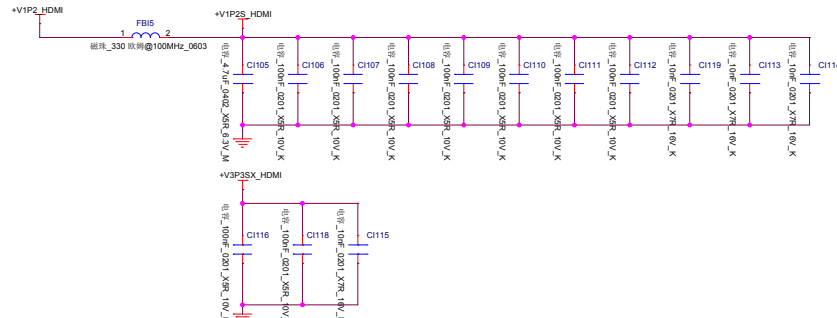
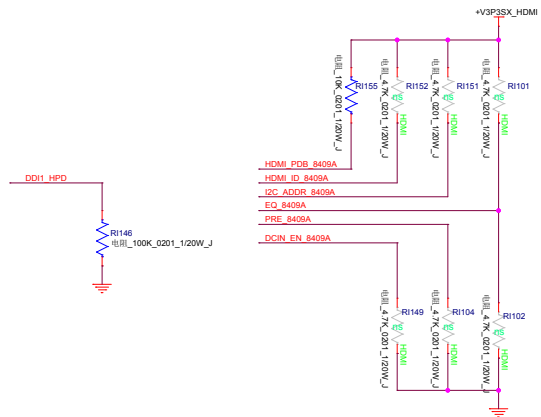
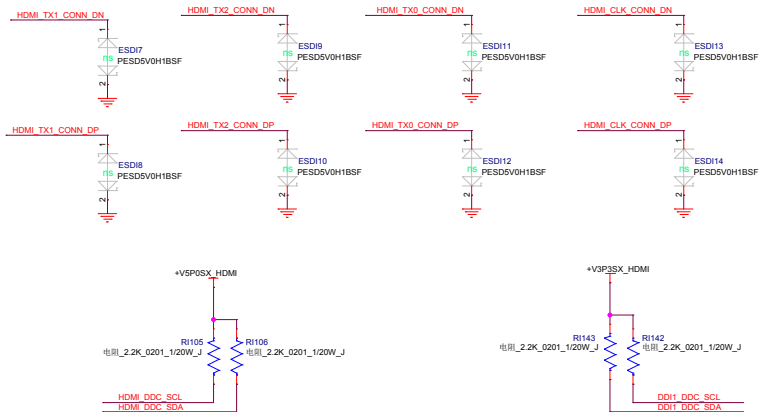
## HDMI CONN



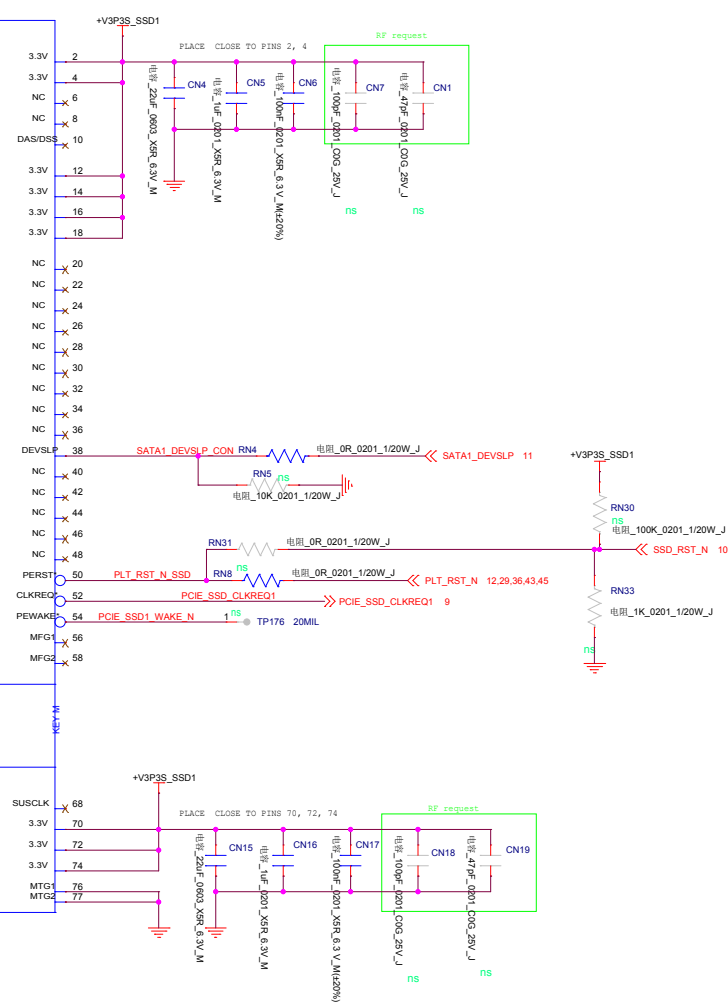
## Signal



ESD

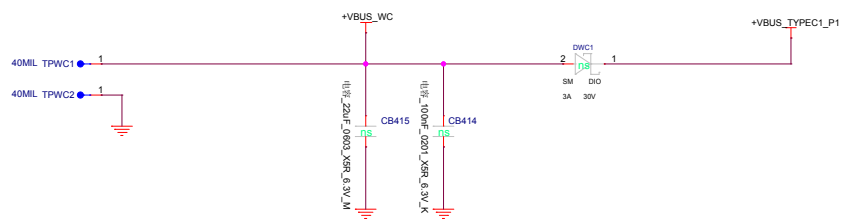


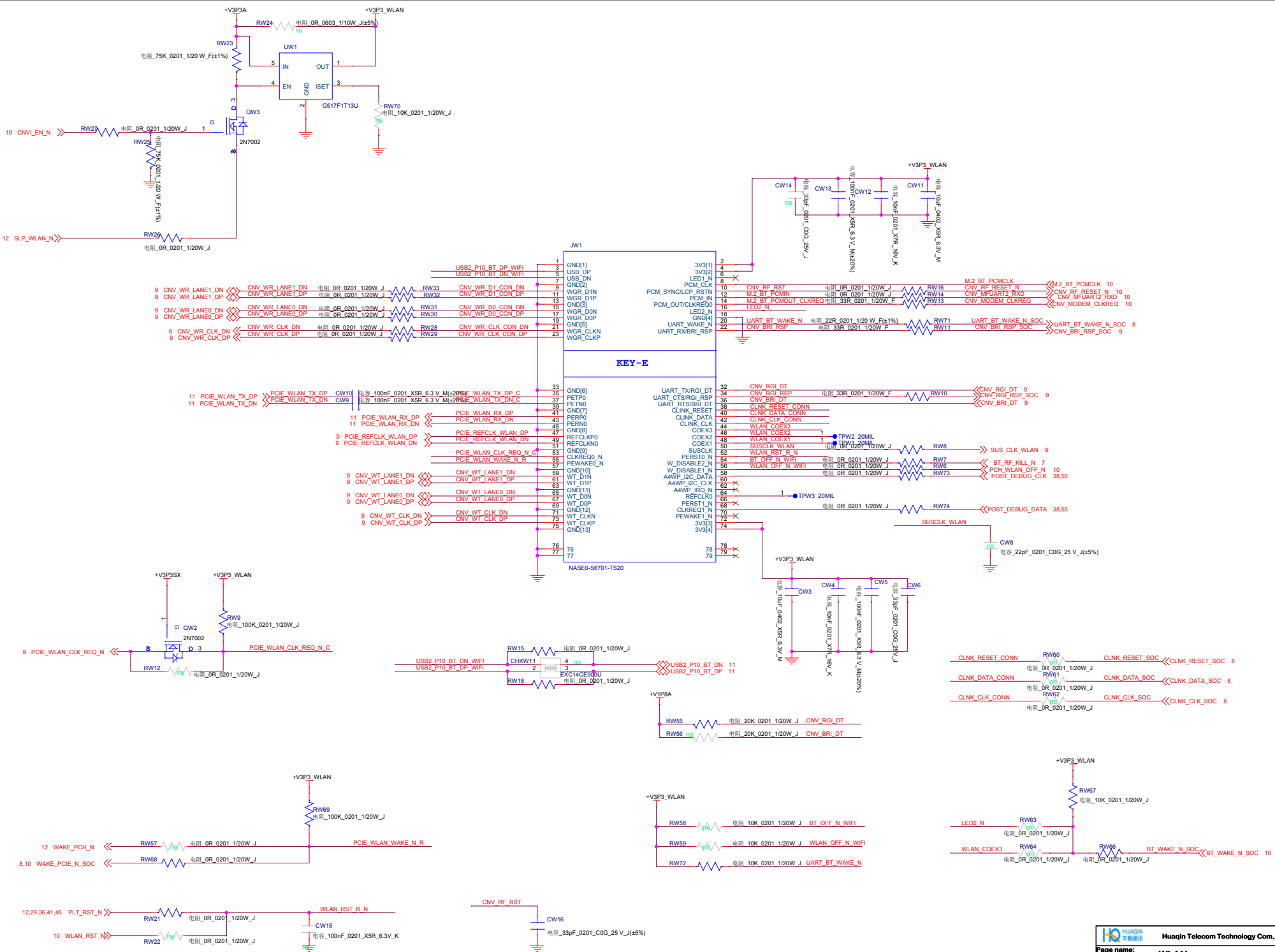
# SSD



MS 需要同时接到CPU GPIO

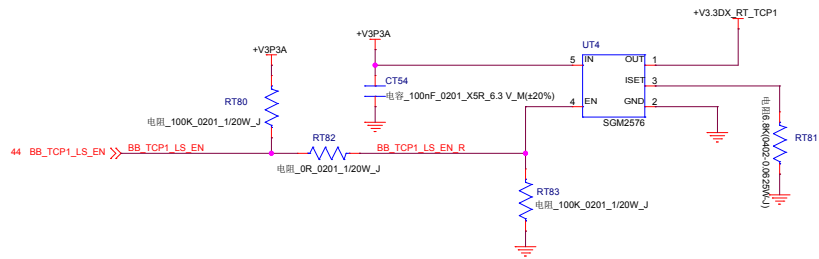
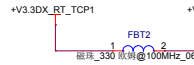
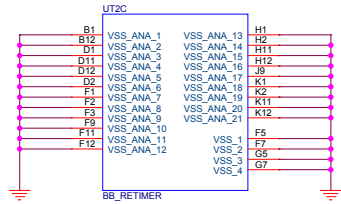
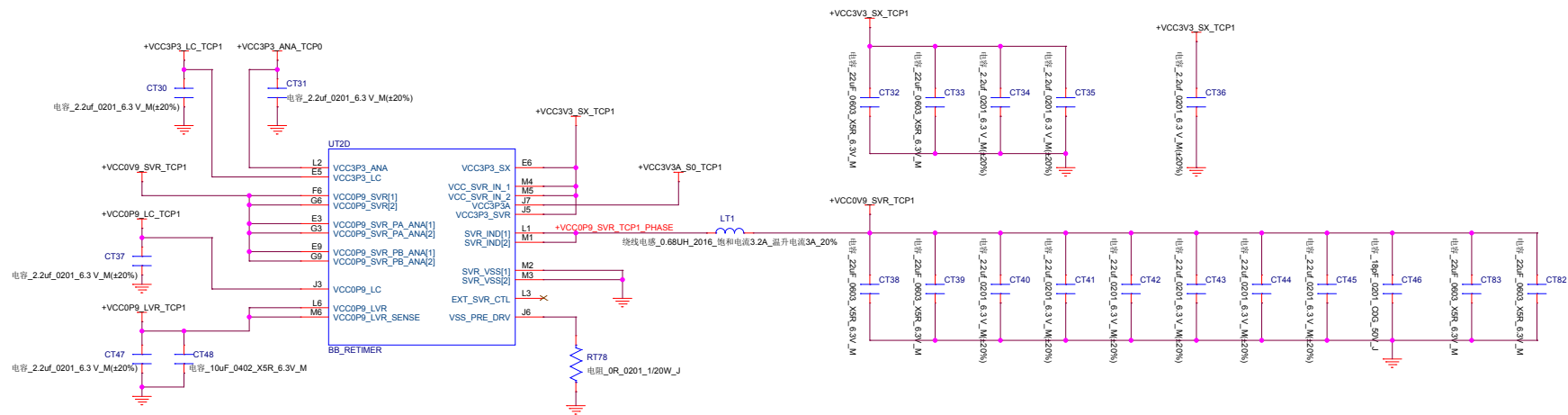
SATA - GND; PCIE - NC



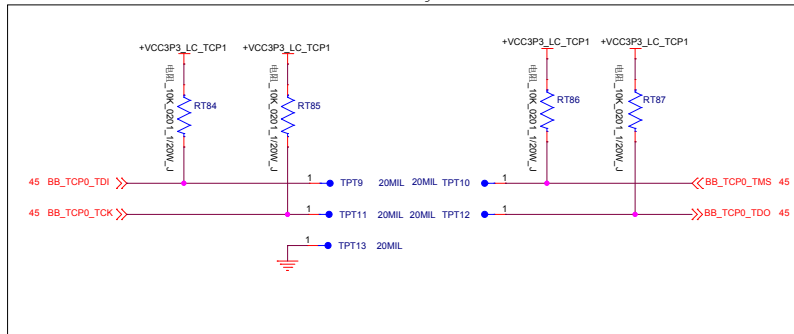




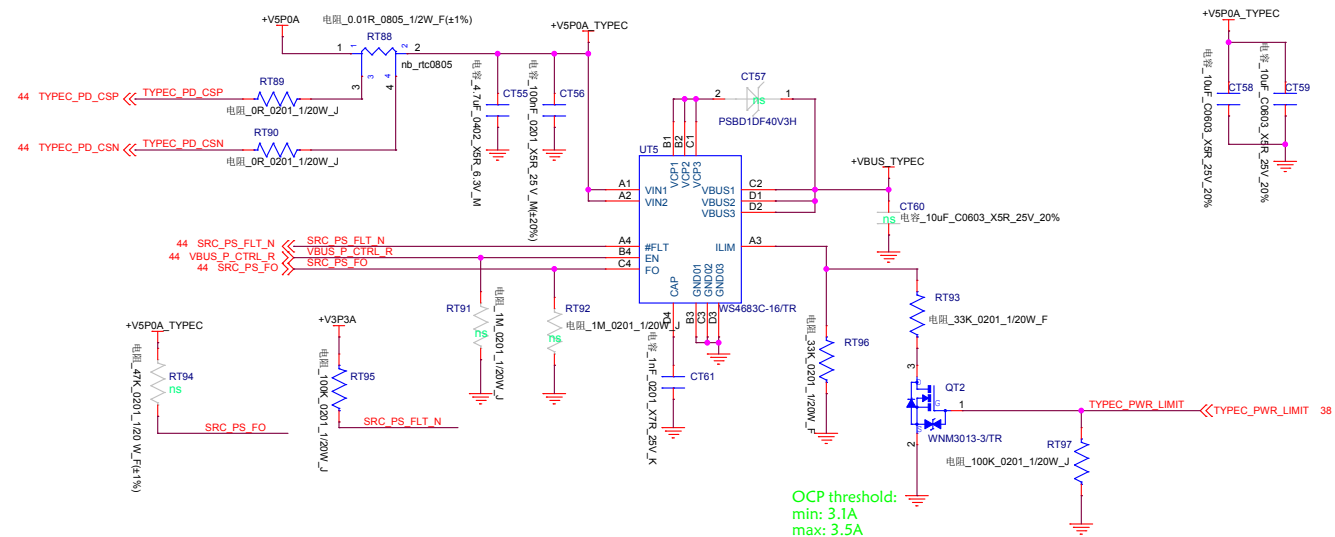




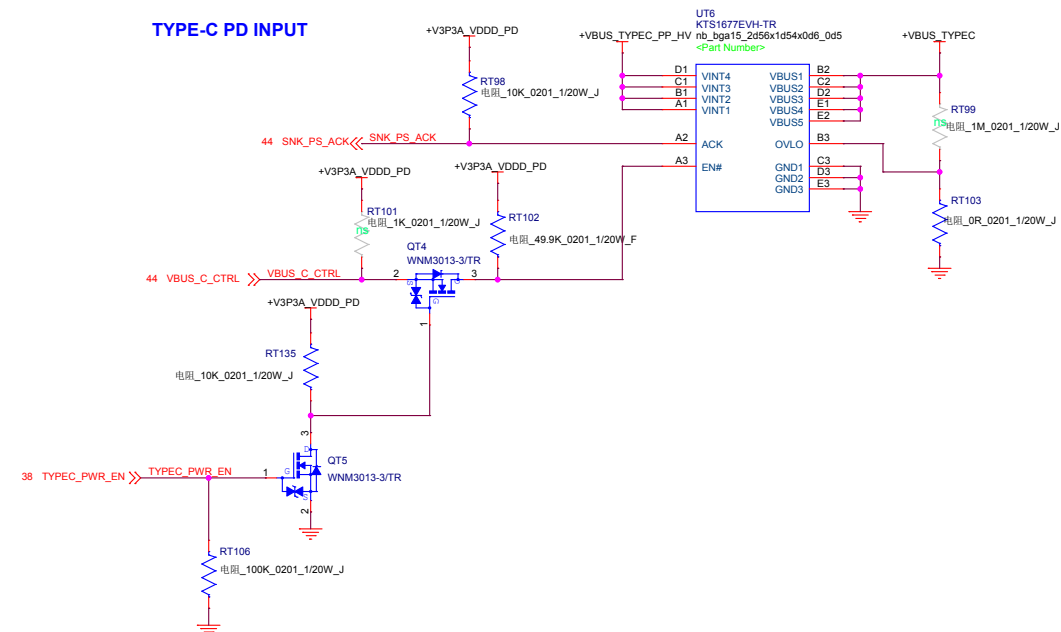
Place together



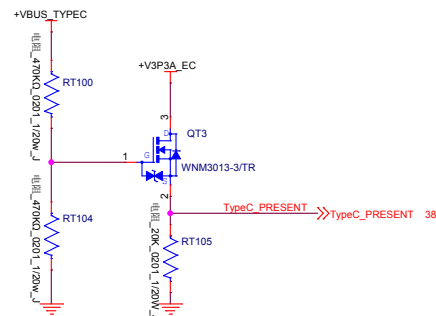
## TYPE-C PD OUTPUT



## TYPE-C PD INPUT

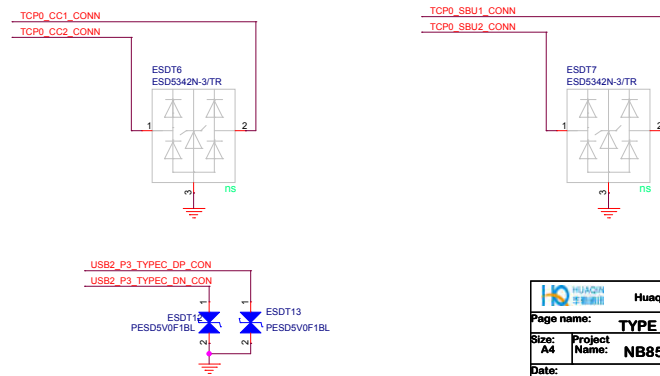
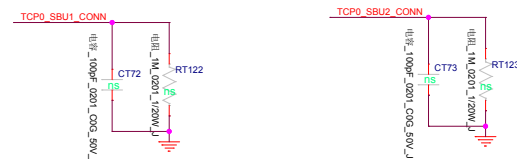
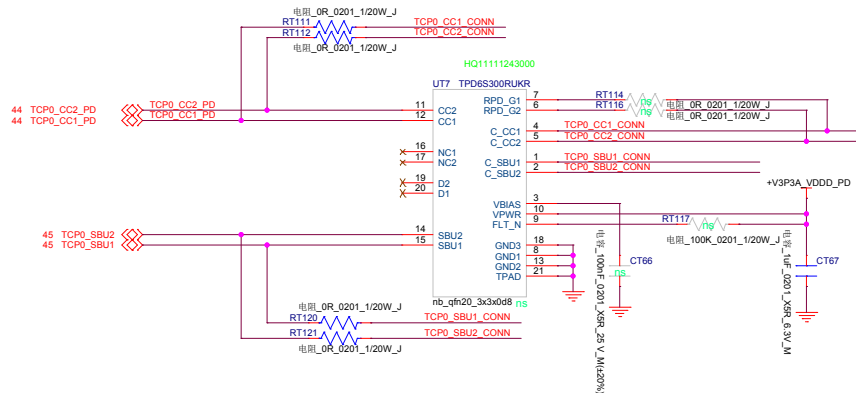
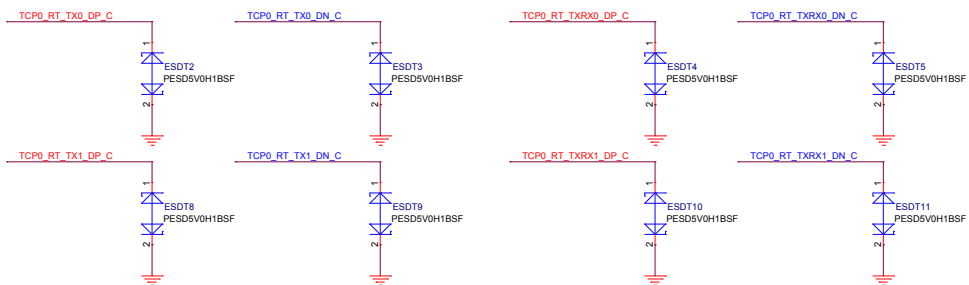
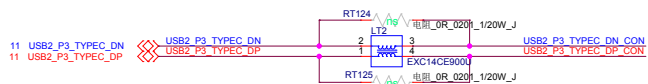
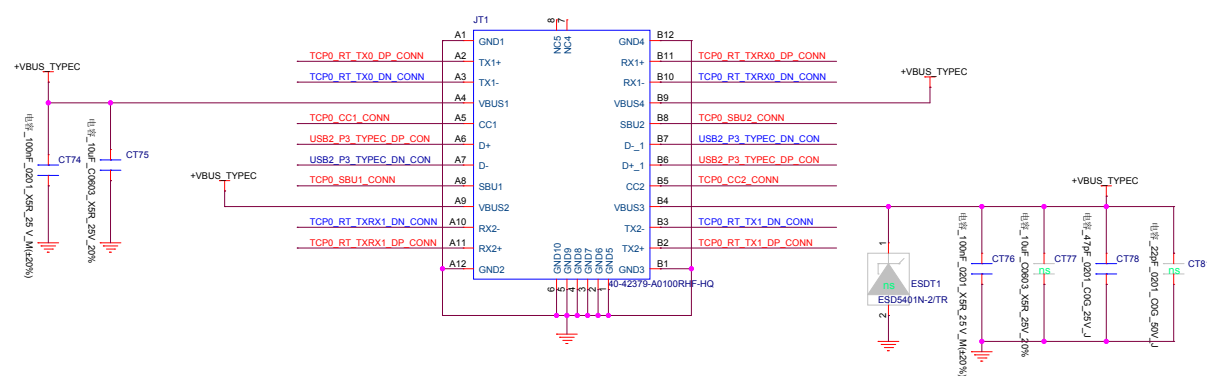
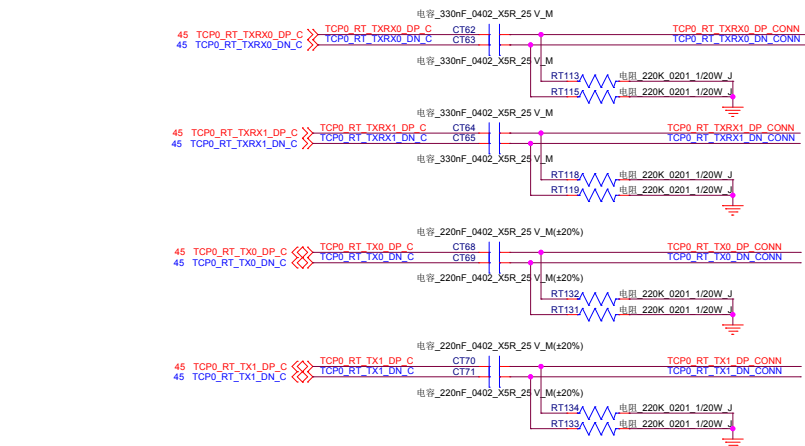


TYPEC-IN detect

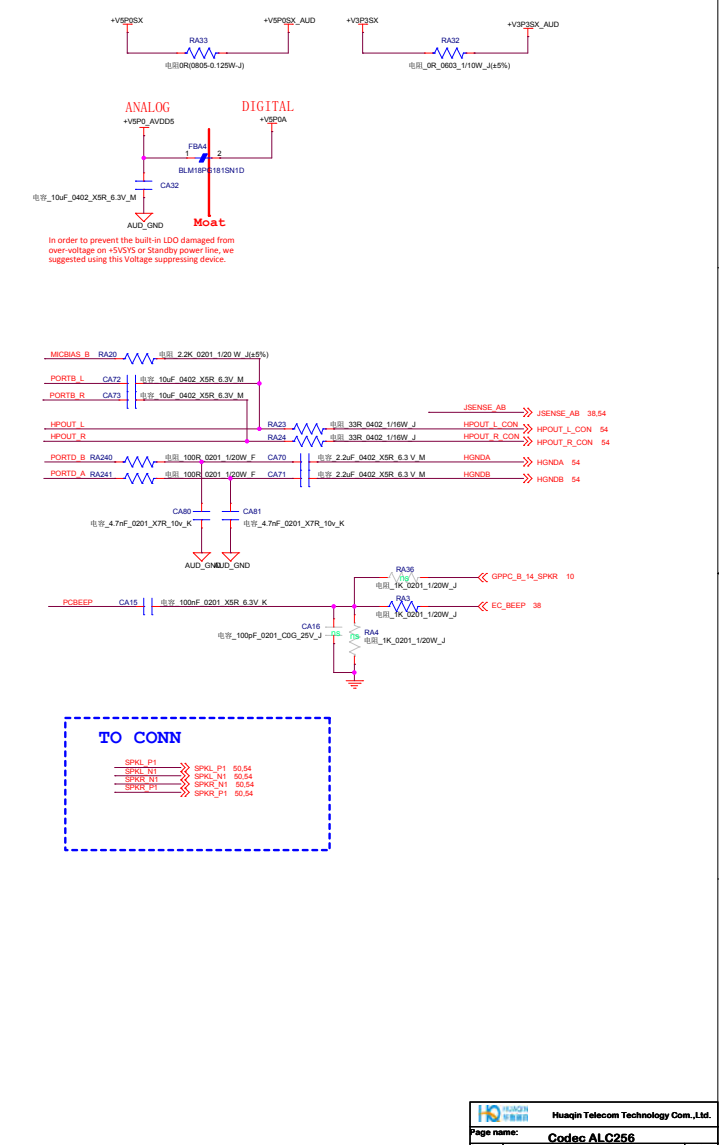
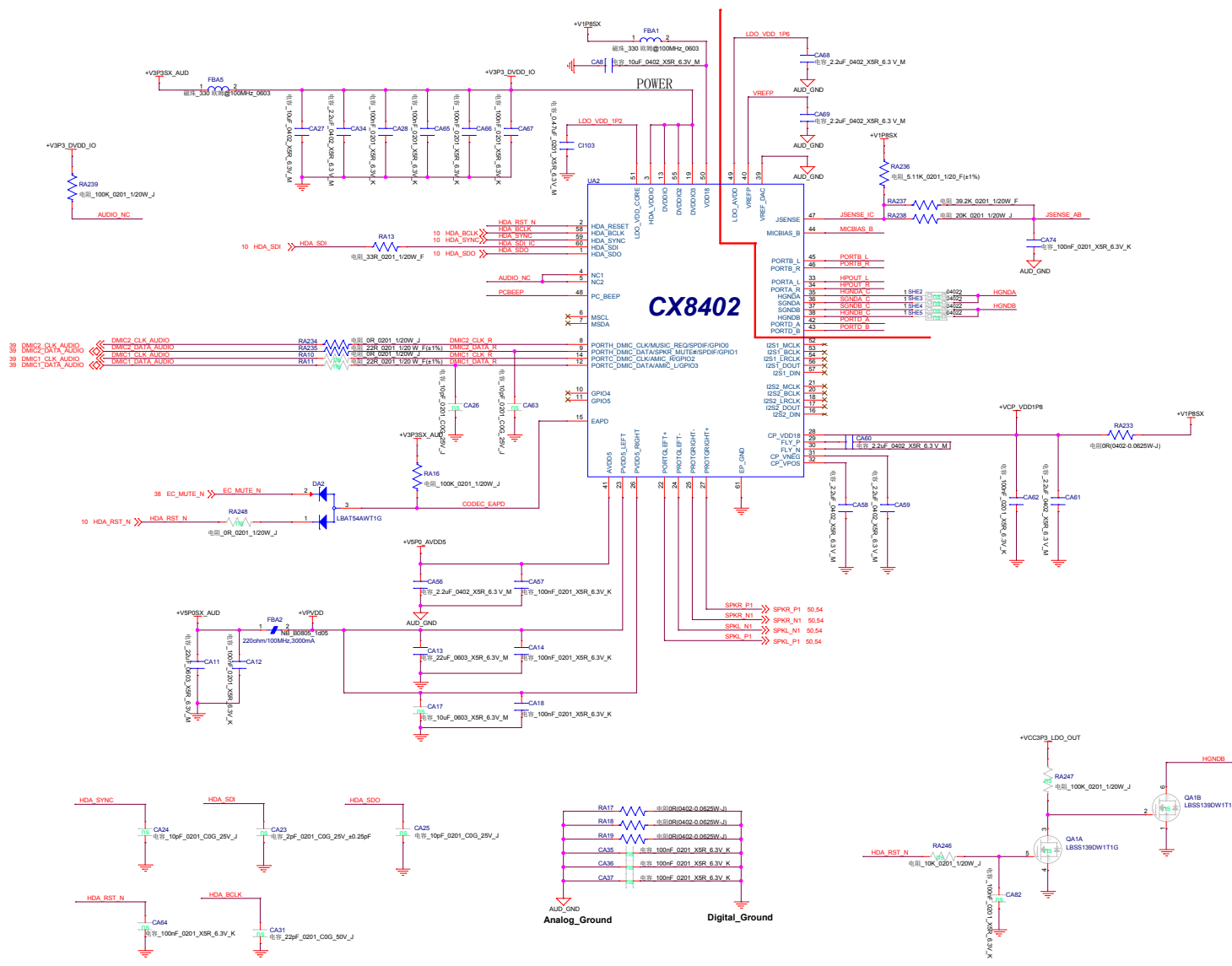


dead battery power on logic

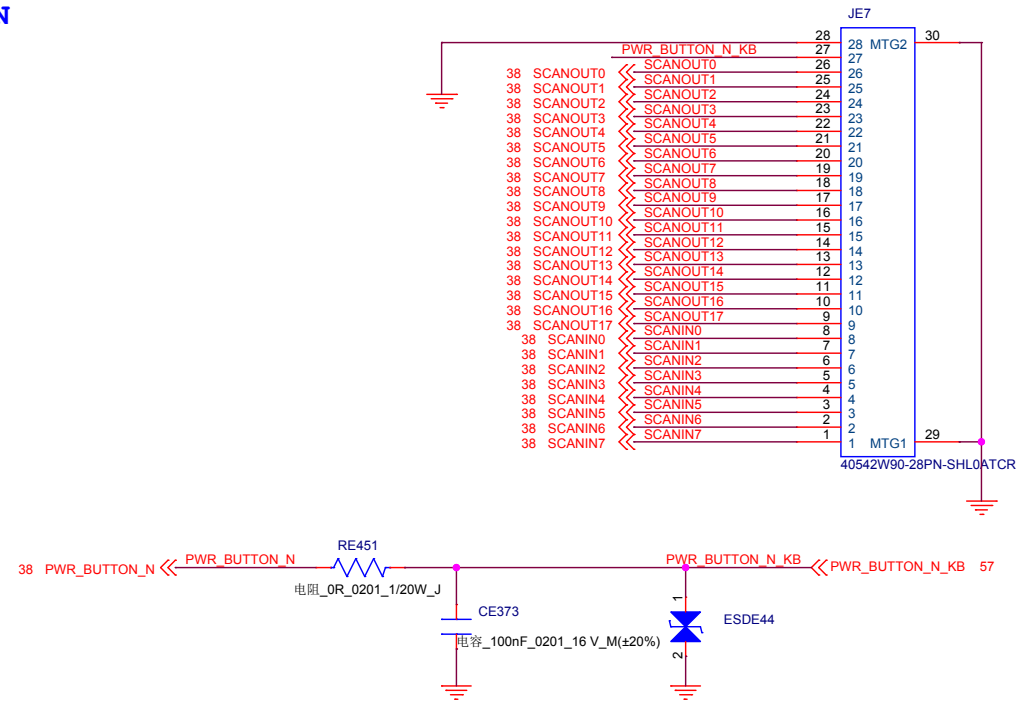
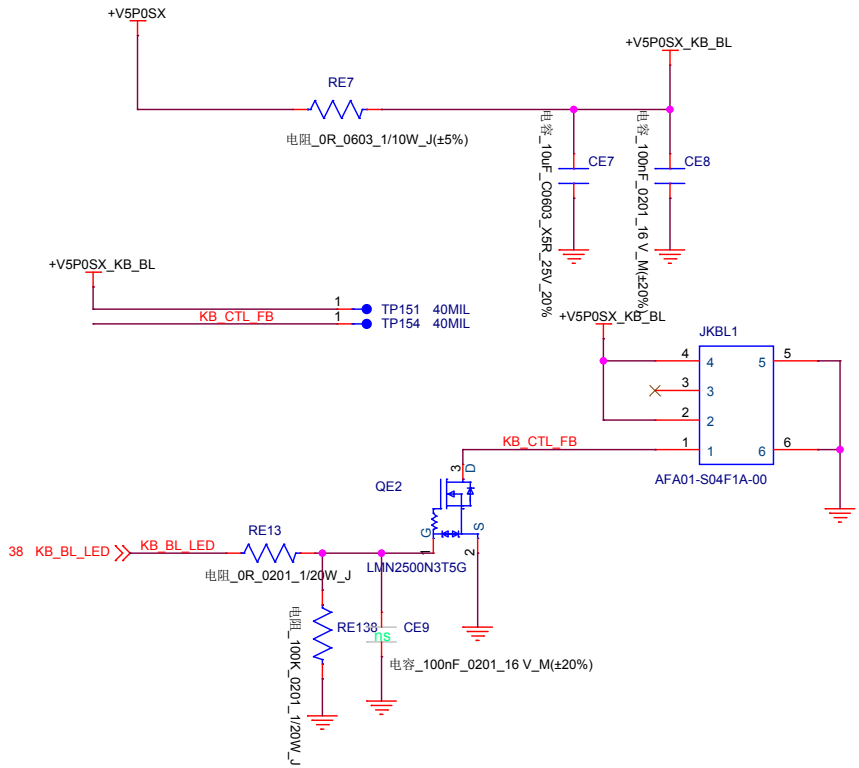
## Discharge



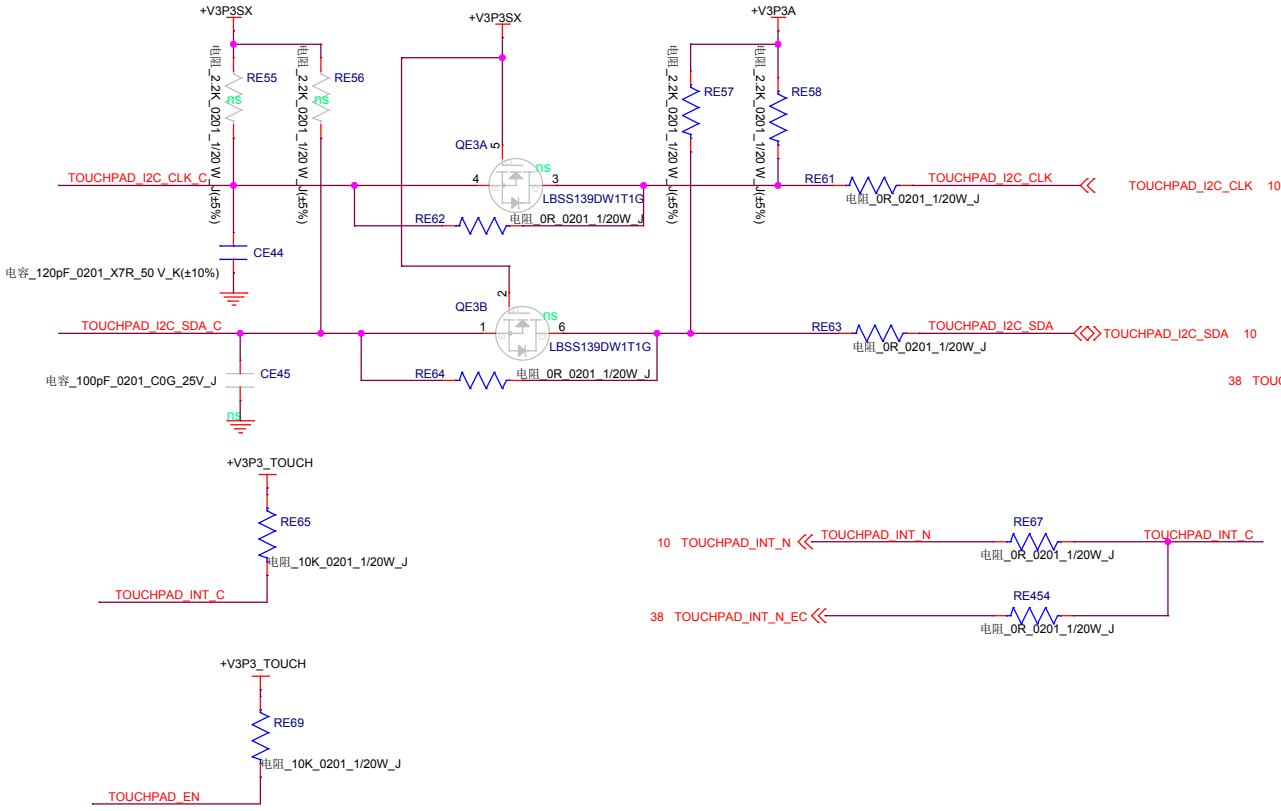




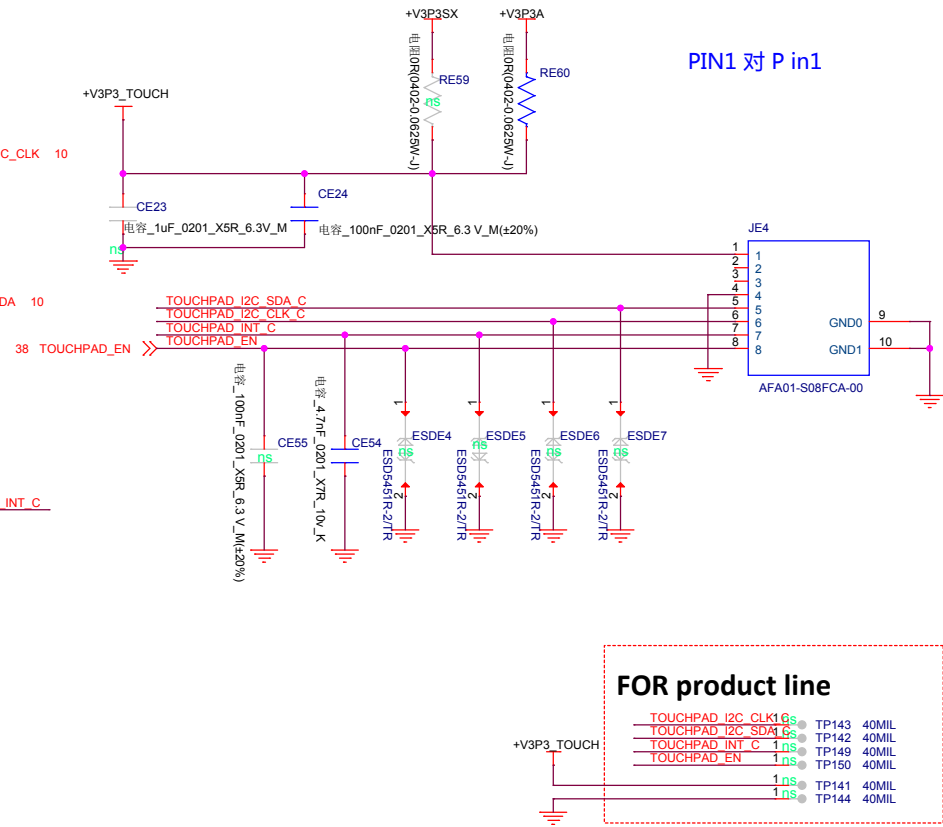
## KB CONN



Touch Pad



Touch Pad CONN

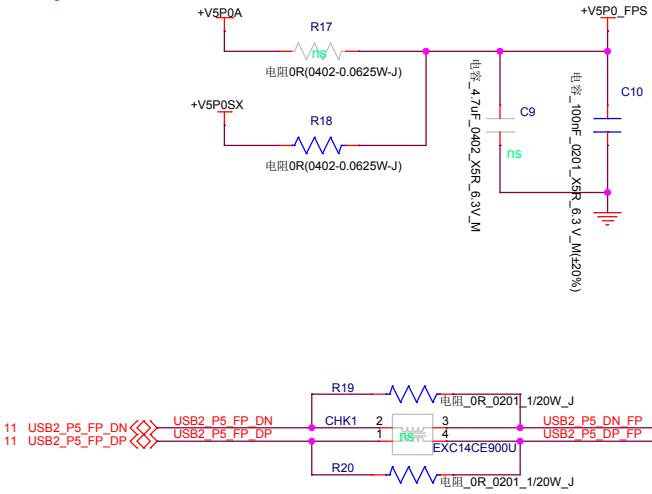


PIN1 对 P in1

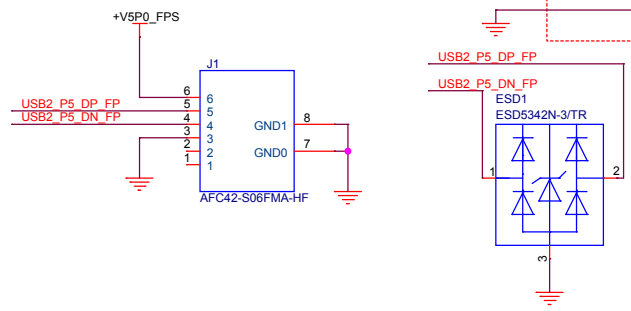
FOR product line

|                    |      |       |       |
|--------------------|------|-------|-------|
| TOUCHPAD_I2C_CLK1  | 1 nS | TP143 | 40MIL |
| TOUCHPAD_I2C_CLK_C | 1 nS | TP142 | 40MIL |
| TOUCHPAD_INT_C     | 1 nS | TP149 | 40MIL |
| TOUCHPAD_EN        | 1 nS | TP150 | 40MIL |
|                    | 1 nS | TP141 | 40MIL |
|                    | 1 nS | TP144 | 40MIL |

Finger Print



Finger Print CONN



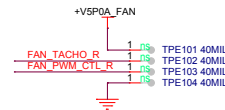
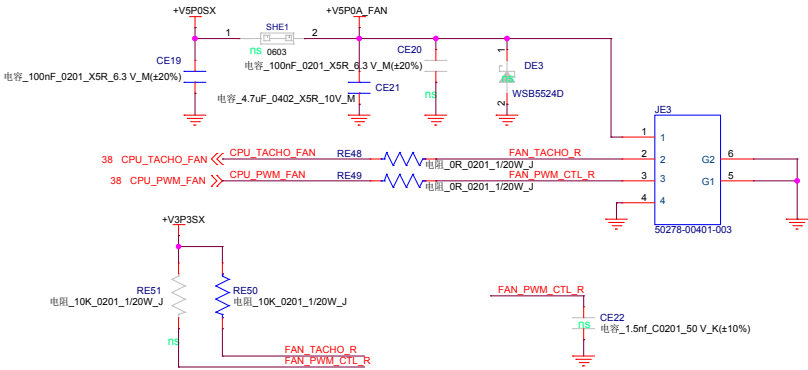
FOR product line

|               |      |       |       |
|---------------|------|-------|-------|
| USB2_P5_DP_FP | 1 nS | TP147 | 40MIL |
| USB2_P5_DN_FP | 1 nS | TP146 | 40MIL |
|               | 1 nS | TP145 | 40MIL |
|               | 1 nS | TP148 | 40MIL |

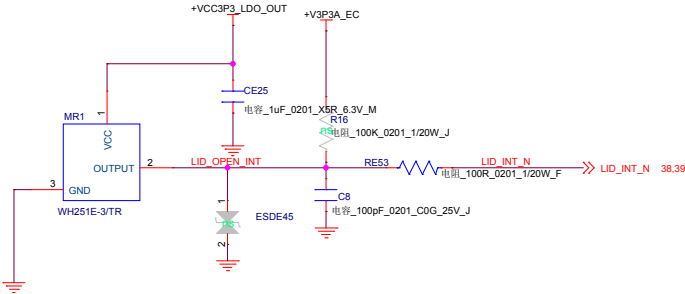
Voice input with LED-NC

FAN CONN

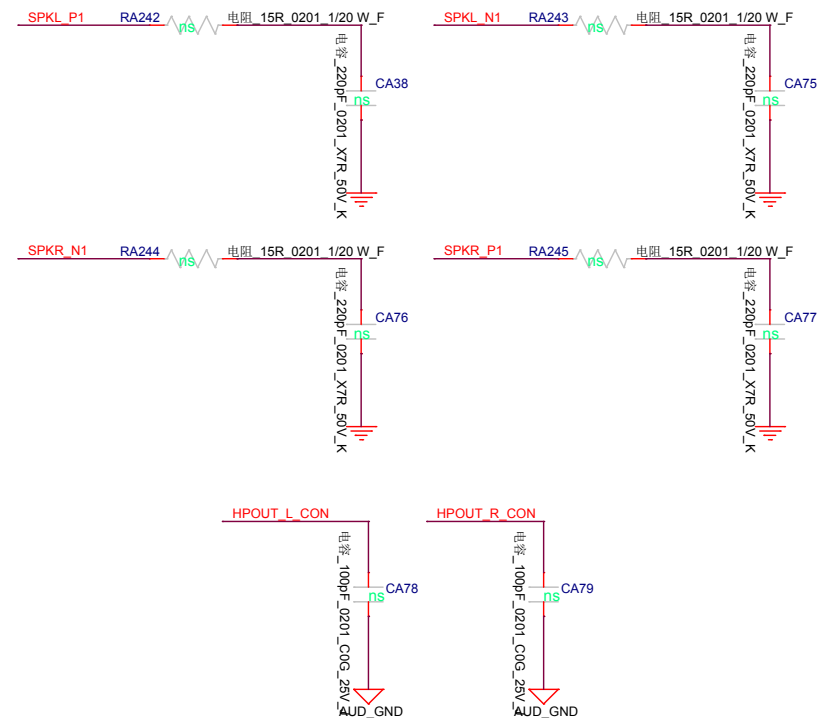
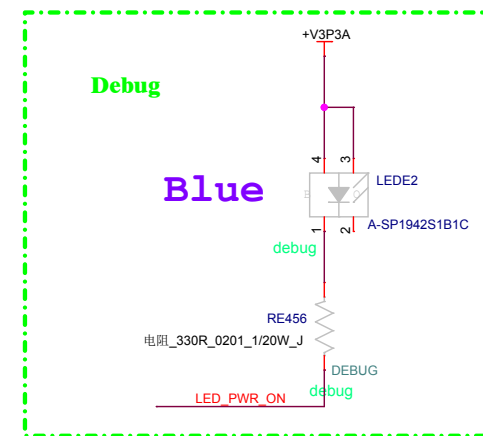
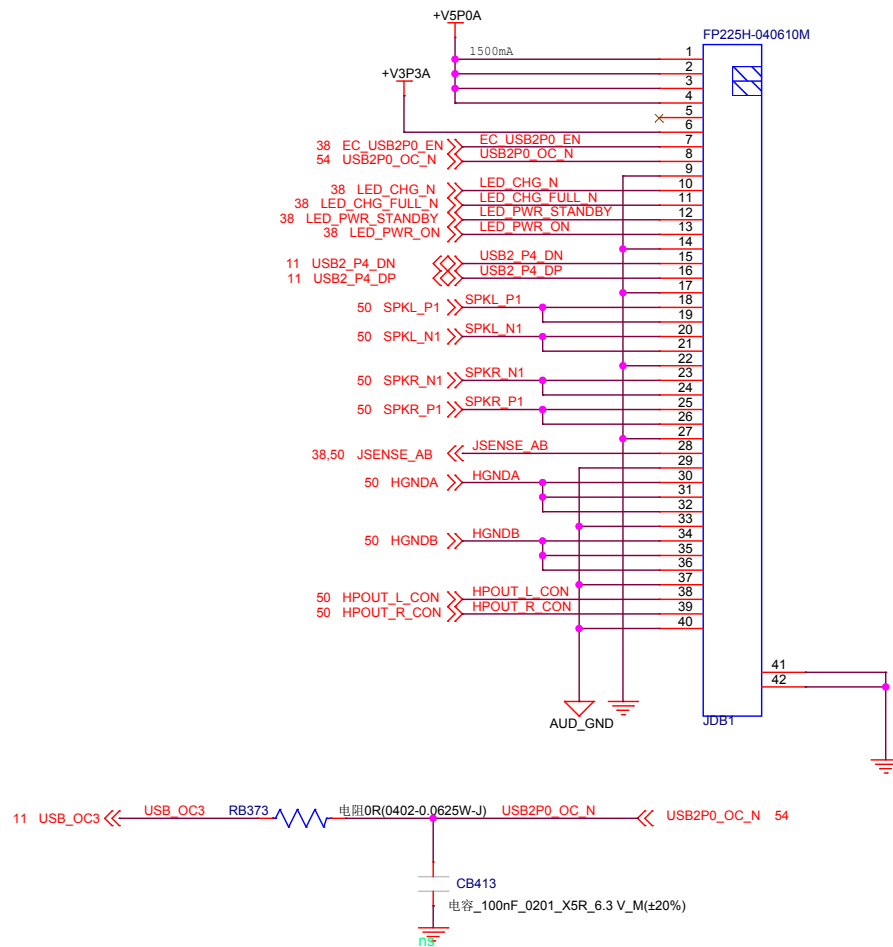
FOR product line



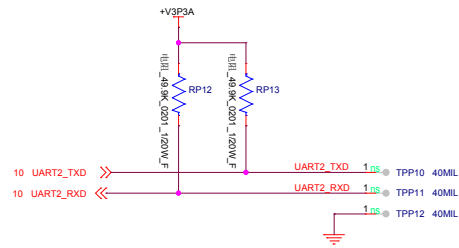
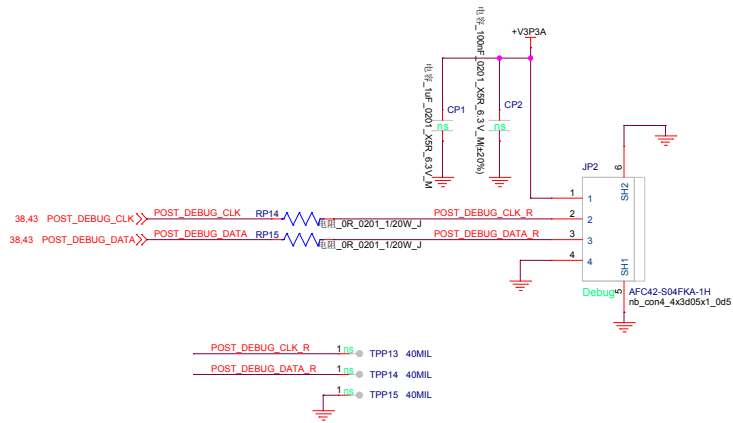
HALL



|                                     |                       |           |  |
|-------------------------------------|-----------------------|-----------|--|
| Huaqin Telecom Technology Com.,Ltd. |                       |           |  |
| Page name:                          | G-SENSOR/FAN/LED/Hall |           |  |
| Size: A4                            | Project Name: NB8511  | REV: V1.0 |  |
| Date: Monday, July 15, 2019         | Sheet: 53             | of 72     |  |

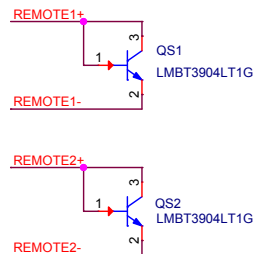
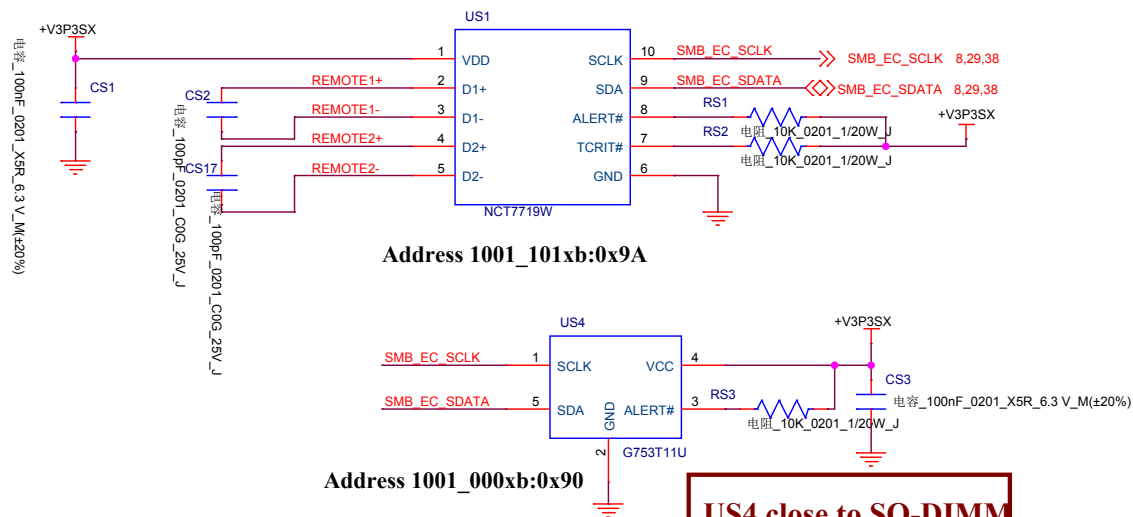


|                                                                                       |                      |                                     |  |
|---------------------------------------------------------------------------------------|----------------------|-------------------------------------|--|
|  |                      | Huaqin Telecom Technology Com.,Ltd. |  |
| Page name: DB CONNECTOR                                                               |                      |                                     |  |
| Size: A4                                                                              | Project Name: NB8511 | REV: V1.0                           |  |
| Date: Monday, July 15, 2019                                                           | Sheet: 54            | of 72                               |  |



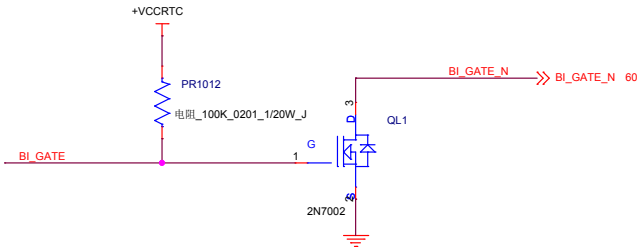
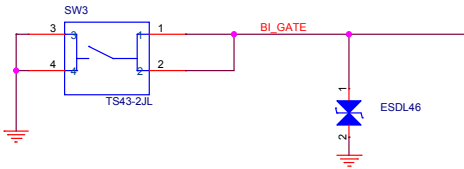
REMOTE1+/-, Trace width/space:10/10 mil,Trace length:<8"  
Connect guard traces to GND on either side of the  
DXP-DXN traces

Close to charger

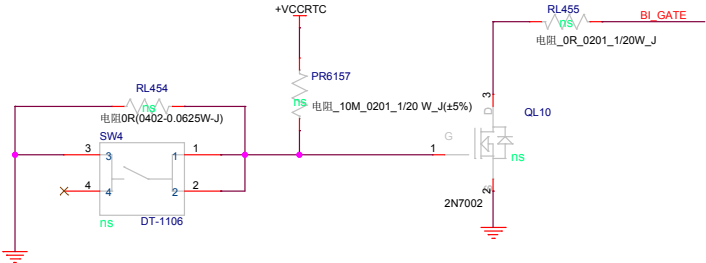


Between CPU and GPU

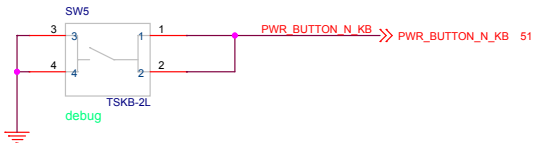
Reset BUTTON



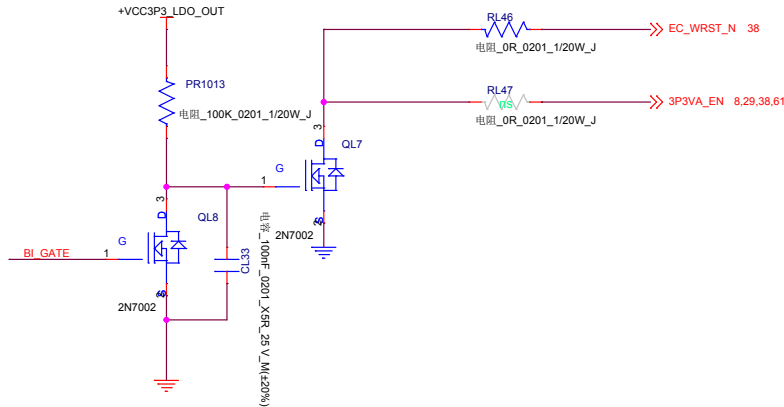
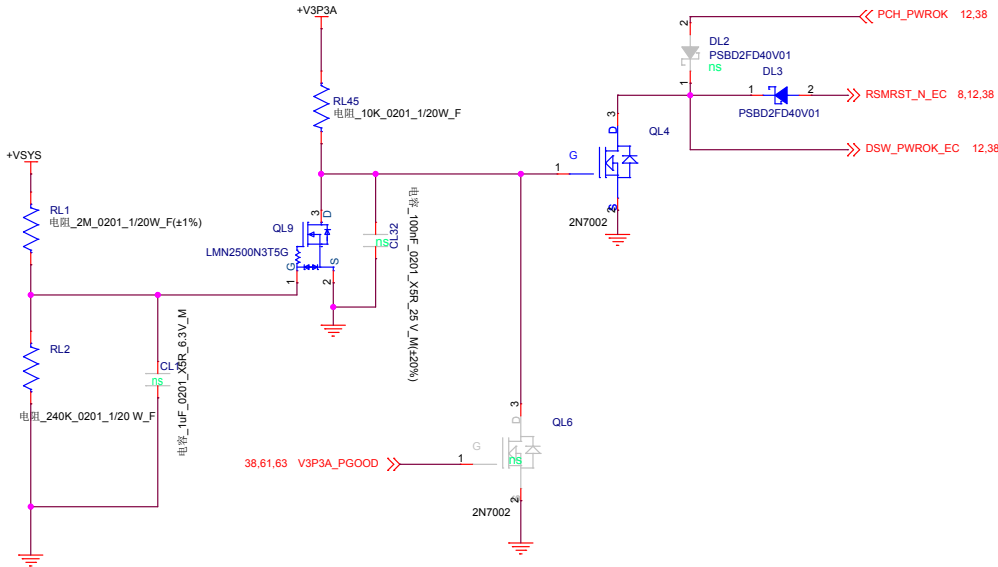
Open door BUTTON



Debug BUTTON



Abnormal PD logic



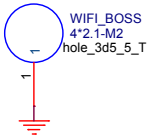
CPU螺母元件 \*4



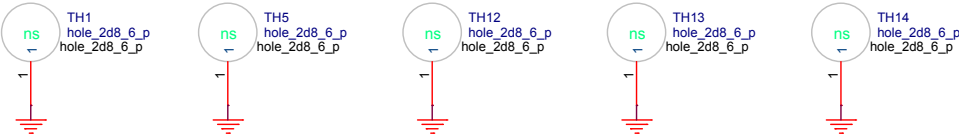
GPU螺母元件 \*2



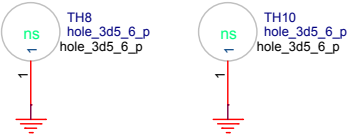
WIFI螺母元件 \*1



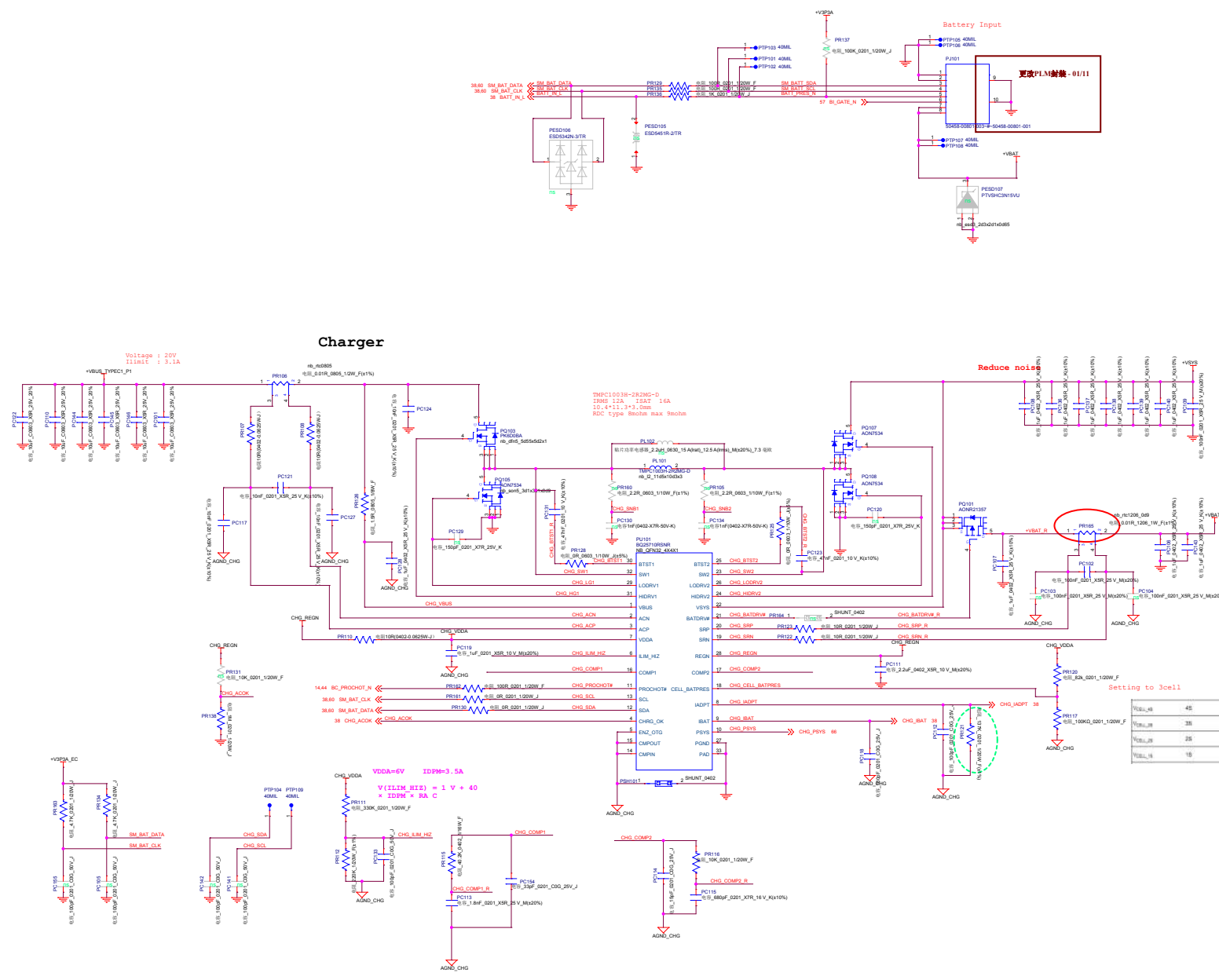
HOLE \*5



HOLE \*2





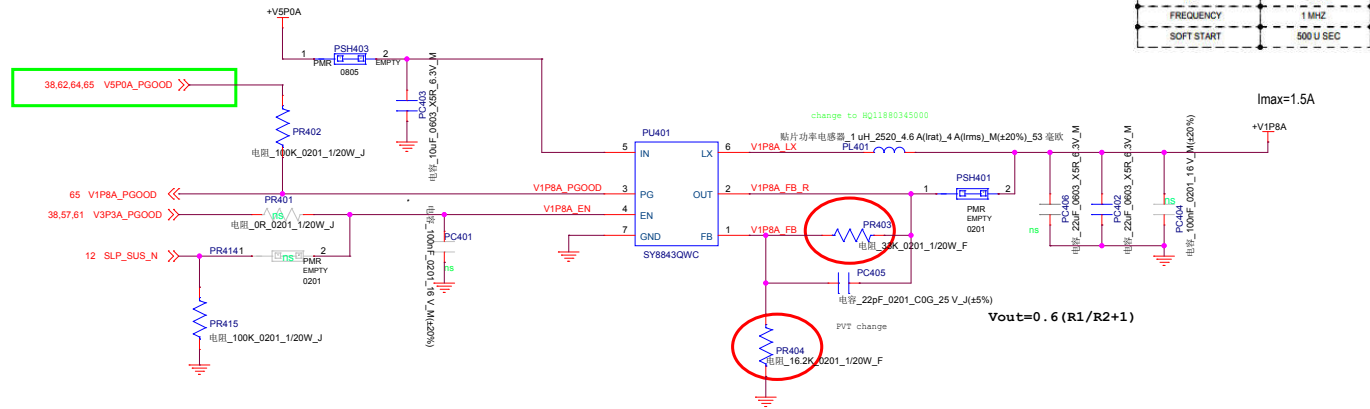


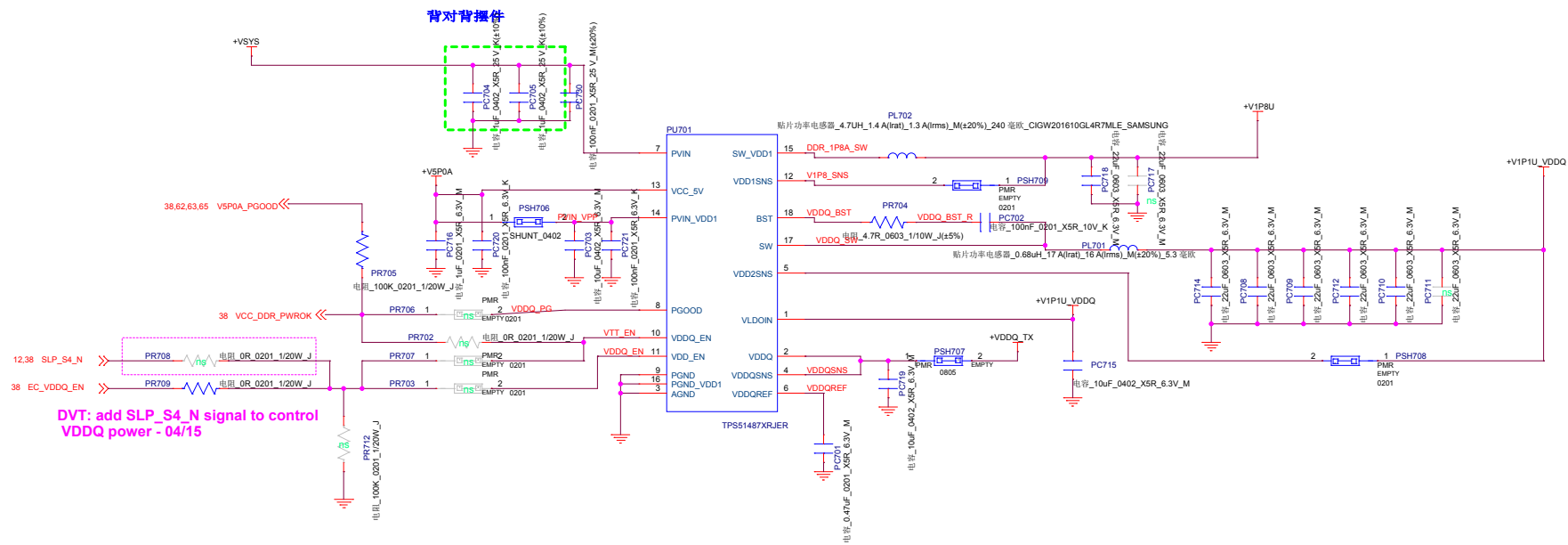
Voltage : battery cell TSD  
Imin : 0.0032A  
Imax : 6.45A  
IIOC : TSD  
OCF : TSD





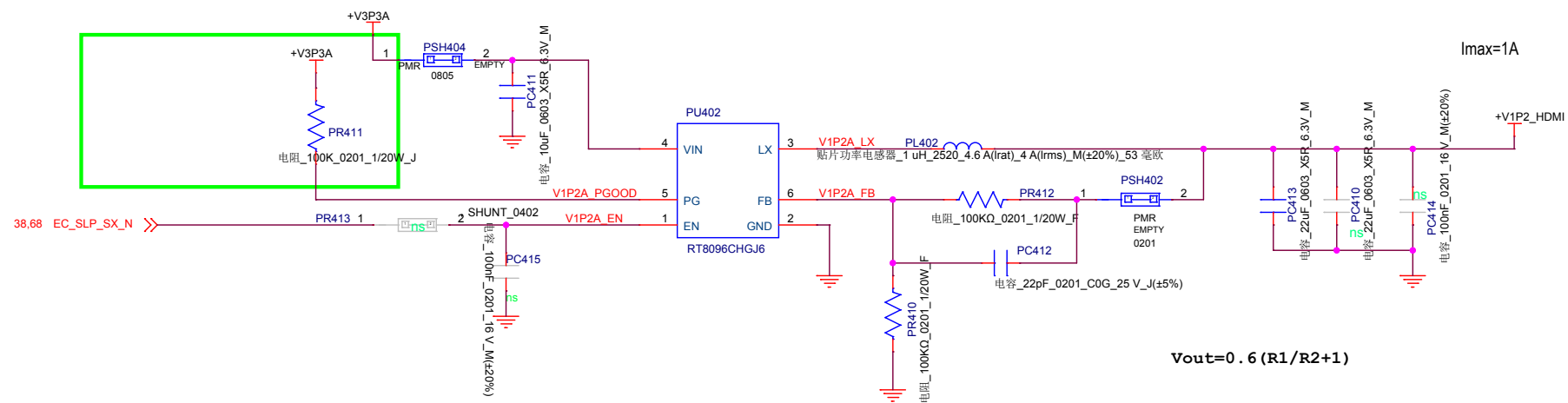
# +V1P8A

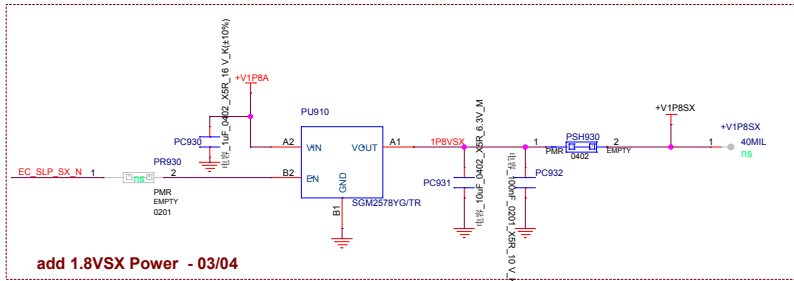




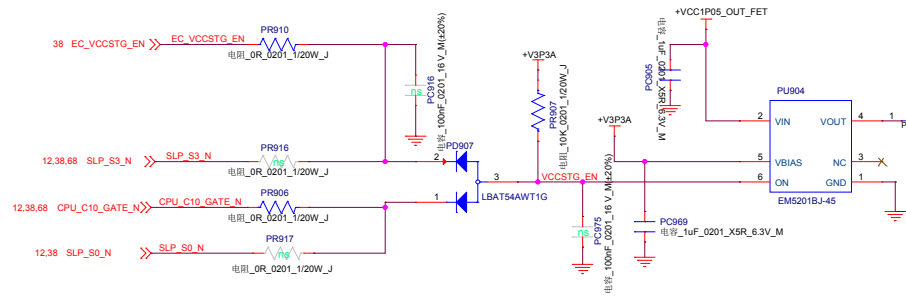




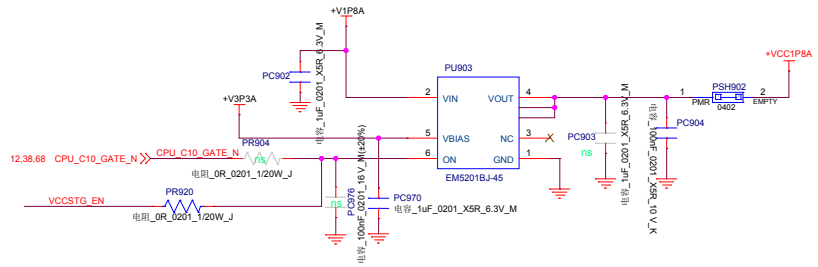




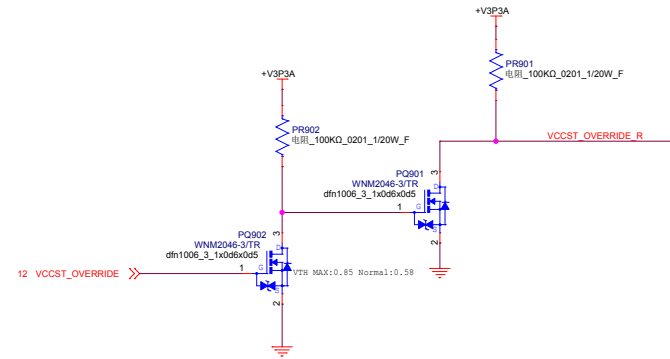
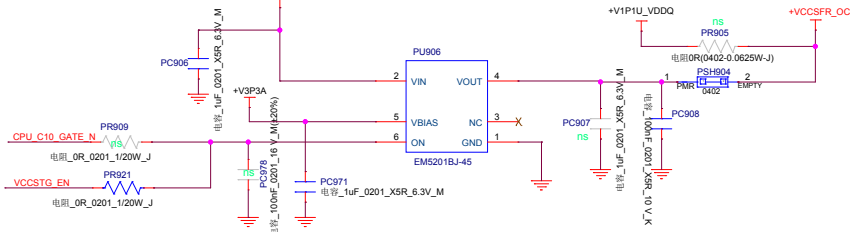
## +VCCSTG\_IO



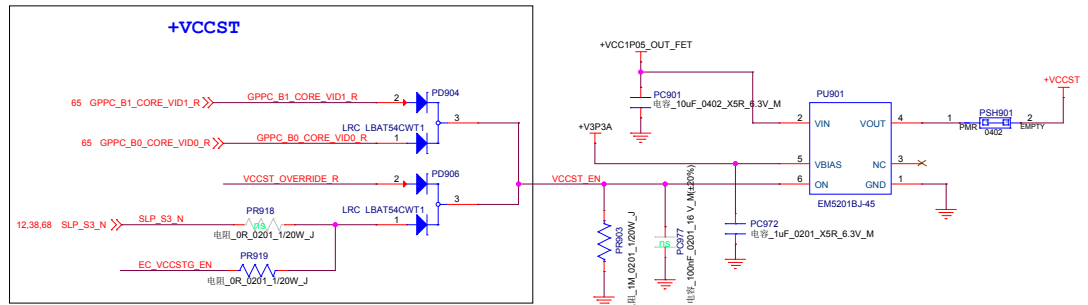
## +VCC1P8A



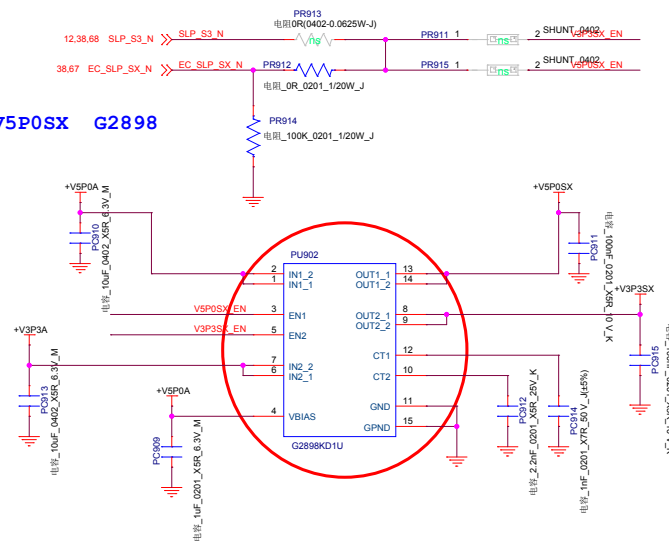
## +VCCSFR\_OC



## +VCCST



## +V3P3SX, +V5P0SX G2898



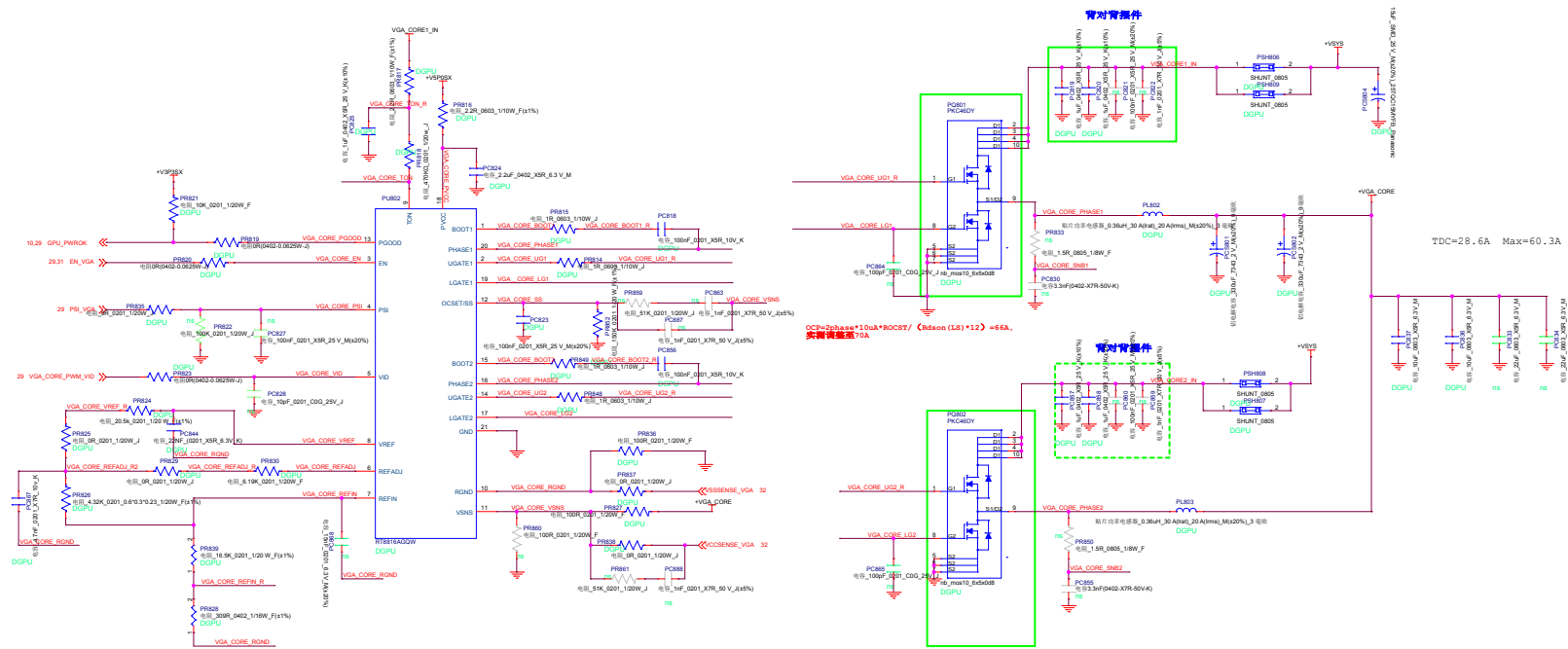


Table 7. Output EDP-Continuous

|                      | NVVD | GPU FBIO           | FB.Total <sup>1</sup> | 1.0V Total <sup>1</sup> | 1.8V Total <sup>2</sup> |
|----------------------|------|--------------------|-----------------------|-------------------------|-------------------------|
|                      | —    | 1.35V <sup>4</sup> | 1.35V <sup>4</sup>    | 1.0V <sup>4</sup>       | 1.8V <sup>4</sup>       |
| Product              | (A)  | (A)                | (A)                   | (A)                     | (A)                     |
| N17S-LG              | 15.4 | 2.5                | 5.0                   | 0.1                     | 0.2                     |
| N17S-G1              | 30.0 | 3.0                | 5.6                   | 0.1                     | 0.3                     |
| N17S-G0 <sup>6</sup> | 27.8 | 3.2                | 5.8                   | 0.2                     | 0.5                     |
| N17S-G2 <sup>6</sup> | 28.6 | 3.2                | 5.8                   | 0.2                     | 0.5                     |

Table 8. Output EDP-Peak

|                      | NVVD | GPU FBIO           | FB.TOTAL <sup>4</sup> | 1.0V Total <sup>1</sup> |
|----------------------|------|--------------------|-----------------------|-------------------------|
|                      | —    | 1.35V <sup>3</sup> | 1.35V <sup>3</sup>    | 1.0V <sup>3</sup>       |
| Product              | (A)  | (A)                | (A)                   | (A)                     |
| N17S-LG              | 48.3 | 2.8                | 5.8                   | 0.2                     |
| N17S-G1              | 60.1 | 3.4                | 6.9                   | 0.2                     |
| N17S-G0 <sup>5</sup> | 42.0 | 3.9                | 7.4                   | 0.3                     |
| N17S-G2 <sup>5</sup> | 60.3 | 3.9                | 7.4                   | 0.3                     |

